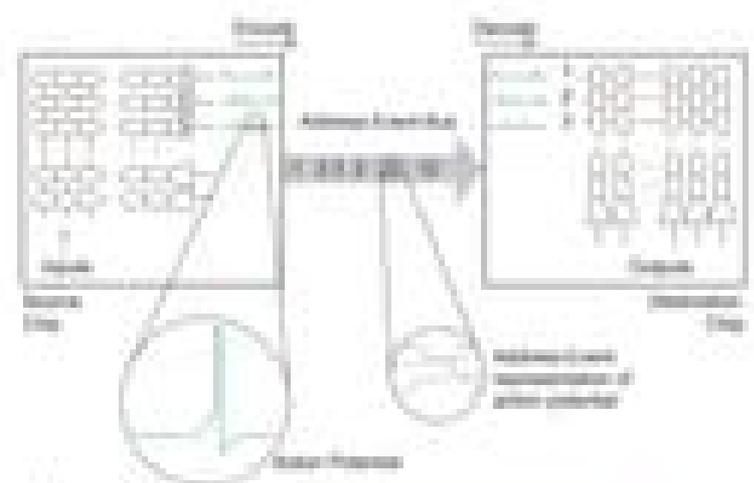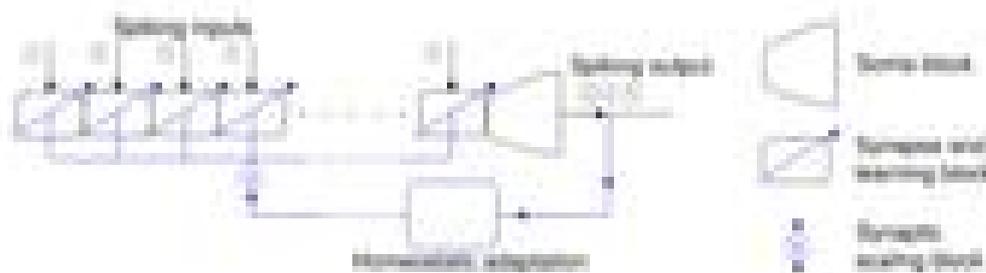# Neuromorphic computing architectures

- Massively parallel collections of non-linear circuits.

- Directly emulate the physics of neural systems.

- Realistic neural and synaptic dynamics

- Distributed, inhomogeneous, imprecise, and noisy.

- Analog computation, digital communication.

- Fault tolerant and mismatch insensitive architectures by design (redundancy and learning).

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Clifford Lane

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Brain-Inspired Computing: From Neuroscience to Neuromorphic Electronics driving new forms of Artificial Intelligence Jonathan Mapelli,Giacomo Indiveri,Angelo Arleo,2022-03-08 <u>Artificial Neural Networks and Machine Learning – ICANN 2024</u> Michael Wand,Kristína Malinovská,Jürgen Schmidhuber,Igor V. Tetko,2024-09-16 The ten volume set LNCS 15016 15025 constitutes the refereed proceedings of the 33rd International Conference on Artificial Neural Networks and Machine Learning ICANN 2024 held in Lugano Switzerland during September 17 20 2024 The 294 full papers and 16 short papers included in these proceedings were carefully reviewed and selected from 764 submissions The papers cover the following topics Part I theory of neural networks and machine learning novel methods in machine learning novel neural architectures neural architecture search self organization neural processes novel architectures for computer vision and fairness in machine learning Part II computer vision classification computer vision object detection computer vision security and adversarial attacks computer vision image enhancement and computer vision 3D methods Part III computer vision anomaly detection computer vision segmentation computer vision pose estimation and tracking computer vision video processing computer vision generative methods and topics in computer vision Part IV brain inspired computing cognitive and computational neuroscience explainable artificial intelligence robotics and reinforcement learning Part V graph neural networks and large language models Part VI multimodality federated learning and time series processing Part VII speech processing natural language processing and language modeling Part VIII biosignal processing in medicine and physiology and medical image processing Part IX human computer interfaces recommender systems environment and climate city planning machine learning in engineering and industry applications in finance artificial intelligence in education social network analysis artificial intelligence and music and software security Part X workshop AI in drug discovery workshop reservoir computing special session accuracy stability and robustness in deep neural networks special session neurorobotics and special session spiking neural networks *Resistive Switching: Oxide Materials, Mechanisms, Devices and Operations* Jennifer Rupp,Daniele Ielmini,Ilia Valov,2021-10-15 This book provides a broad examination of redox based resistive switching memories ReRAM a promising technology for novel types of nanoelectronic devices according to the International Technology Roadmap for Semiconductors and the materials and physical processes used in these ionic transport based switching devices It covers defect kinetic models for switching ReRAM deposition fabrication methods tuning thin film microstructures and material device characterization and modeling A slate of world renowned authors address the influence of type of ionic carriers their mobility the role of the local and chemical composition and environment and facilitate readers understanding of the effects of composition and structure at different length scales e g crystalline vs amorphous phases impact of extended defects such as dislocations and grain boundaries ReRAMs show outstanding potential for scaling down to the atomic level fast operation in the nanosecond range low power consumption and non volatile storage The book is ideal

for materials scientists and engineers concerned with novel types of nanoelectronic devices such as memories memristors and switches for logic and neuromorphic computing circuits beyond the von Neumann concept   <u>Intelligent Systems and Applications</u> Kohei Arai,2025-09-22 The 11th Intelligent Systems Conference IntelliSys 2025 held in Amsterdam The Netherlands from 28 29 August 2025 brought together researchers practitioners and experts from around the world to share advancements in intelligent technologies Conducted in a hybrid format the conference facilitated global collaboration and participation This volume presents a curated selection of 169 peer reviewed papers from a total of 470 submissions covering key areas such as Artificial Intelligence Computer Vision Robotics and Intelligent Systems The contributions reflect the latest research trends practical applications and emerging challenges in these domains We hope that these proceedings serve as a valuable resource for researchers practitioners and students and that they inspire future work and collaborations in the field of intelligent systems   **Proceedings of the TEPEN International Workshop on Fault Diagnostic and Prognostic** Zuolu Wang,Kai Zhang,Ke Feng,Yuandong Xu,Wenxian Yang,2024-10-19 This book gathers the latest advances innovations and applications in the field of efficiency and performance engineering as presented by leading international researchers and engineers at the TEPEN International Workshop on Fault Diagnostics and Prognostics TEPEN IWFDP held in Qingdao China on May 8 11 2024 Topics include machine and structural health monitoring non destructive testing and fault detection diagnostic and prognostic for both operational and manufacturing processes maintenance optimization and asset management smart metamaterials and metastructures artificial intelligent and machine learning The contributions which are selected through a rigorous international peer review process share exciting ideas that spur novel research directions and foster new multidisciplinary collaborations   **Springer Handbook of Semiconductor Devices** Massimo Rudan,Rossella Brunetti,Susanna Reggiani,2022-11-10 This Springer Handbook comprehensively covers the topic of semiconductor devices embracing all aspects from theoretical background to fabrication modeling and applications Nearly 100 leading scientists from industry and academia were selected to write the handbook s chapters which were conceived for professionals and practitioners material scientists physicists and electrical engineers working at universities industrial R D and manufacturers Starting from the description of the relevant technological aspects and fabrication steps the handbook proceeds with a section fully devoted to the main conventional semiconductor devices like e g bipolar transistors and MOS capacitors and transistors used in the production of the standard integrated circuits and the corresponding physical models In the subsequent chapters the scaling issues of the semiconductor device technology are addressed followed by the description of novel concept based semiconductor devices The last section illustrates the numerical simulation methods ranging from the fabrication processes to the device performances Each chapter is self contained and refers to related topics treated in other chapters when necessary so that the reader interested in a specific subject can easily identify a personal reading path through the vast contents of the handbook   **Neuroscience, computing, performance, and benchmarks: Why it**

matters to neuroscience how fast we can compute Felix Schürmann,Omar Awile,James Courtney Knight,Thomas Nowotny,James B. Aimone,Markus Diesmann,2023-04-26 *Neuromorphic Intelligence* Shuangming Yang,Badong Chen,2024-05-14 This book provides a valuable resource on the design of neuromorphic intelligence which serves as a computational foundation for building compact and low power brain inspired intelligent systems The book introduces novel spiking neural network learning algorithms including spike based learning based on the multi compartment model and spike based learning with information theory These offer important insights and academic value for readers to grasp the latest advances in neural inspired learning Additionally the book presents insights and approaches to the design of scalable neuromorphic architectures which are crucial foundations for achieving highly cognitive and energy efficient computing systems Furthermore the book introduces representative large scale neuromorphic systems and reviews several recently implemented large scale digital neuromorphic systems by the authors providing corresponding application scenarios

Neuromorphic Computing Principles and Organization Abderazek Ben Abdallah,Khanh N. Dang,2022-05-31 This book focuses on neuromorphic computing principles and organization and how to build fault tolerant scalable hardware for large and medium scale spiking neural networks with learning capabilities In addition the book describes in a comprehensive way the organization and how to design a spike based neuromorphic system to perform network of spiking neurons communication computing and adaptive learning for emerging AI applications The book begins with an overview of neuromorphic computing systems and explores the fundamental concepts of artificial neural networks Next we discuss artificial neurons and how they have evolved in their representation of biological neuronal dynamics Afterward we discuss implementing these neural networks in neuron models storage technologies inter neuron communication networks learning and various design approaches Then comes the fundamental design principle to build an efficient neuromorphic system in hardware The challenges that need to be solved toward building a spiking neural network architecture with many synapses are discussed Learning in neuromorphic computing systems and the major emerging memory technologies that promise neuromorphic computing are then given A particular chapter of this book is dedicated to the circuits and architectures used for communication in neuromorphic systems In particular the Network on Chip fabric is introduced for receiving and transmitting spikes following the Address Event Representation AER protocol and the memory accessing method In addition the interconnect design principle is covered to help understand the overall concept of on chip and off chip communication Advanced on chip interconnect technologies including si photonic three dimensional interconnects and fault tolerant routing algorithms are also given The book also covers the main threats of reliability and discusses several recovery methods for multicore neuromorphic systems This is important for reliable processing in several embedded neuromorphic applications A reconfigurable design approach that supports multiple target applications via dynamic reconfigurability network topology independence and network expandability is also described in the subsequent chapters The book ends with a case study about

a real hardware software design of a reliable three dimensional digital neuromorphic processor geared explicitly toward the 3D ICs biological brain s three dimensional structure The platform enables high integration density and slight spike delay of spiking networks and features a scalable design We present methods for fault detection and recovery in a neuromorphic system as well Neuromorphic Computing Principles and Organization is an excellent resource for researchers scientists graduate students and hardware software engineers dealing with the ever increasing demands on fault tolerance scalability and low power consumption It is also an excellent resource for teaching advanced undergraduate and graduate students about the fundamentals concepts organization and actual hardware software design of reliable neuromorphic systems with learning and fault tolerance capabilities   Neuromorphic Engineering Systems and Applications André van Schaik,Tobi Delbruck,Jennifer Hasler,2015-07-05 Neuromorphic engineering has just reached its 25th year as a discipline In the first two decades neuromorphic engineers focused on building models of sensors such as silicon cochleas and retinas and building blocks such as silicon neurons and synapses These designs have honed our skills in implementing sensors and neural networks in VLSI using analog and mixed mode circuits Over the last decade the address event representation has been used to interface devices and computers from different designers and even different groups This facility has been essential for our ability to combine sensors neural networks and actuators into neuromorphic systems More recently several big projects have emerged to build very large scale neuromorphic systems The Telluride Neuromorphic Engineering Workshop since 1994 and the CapoCaccia Cognitive Neuromorphic Engineering Workshop since 2009 have been instrumental not only in creating a strongly connected research community but also in introducing different groups to each other s hardware Many neuromorphic systems are first created at one of these workshops With this special research topic we showcase the state of the art in neuromorphic systems   **Analog Spiking Neuromorphic Circuits and Systems for Brain- and Nanotechnology-inspired Cognitive Computing** Xinyu Wu,2016 Human society is now facing grand challenges to satisfy the growing demand for computing power at the same time sustain energy consumption By the end of CMOS technology scaling innovations are required to tackle the challenges in a radically different way Inspired by the emerging understanding of the computing occurring in a brain and nanotechnology enabled biological plausible synaptic plasticity neuromorphic computing architectures are being investigated Such a neuromorphic chip that combines CMOS analog spiking neurons and nanoscale resistive random access memory RRAM using as electronics synapses can provide massive neural network parallelism high density and online learning capability and hence paves the path towards a promising solution to future energy efficient real time computing systems However existing silicon neuron approaches are designed to faithfully reproduce biological neuron dynamics and hence they are incompatible with the RRAM synapses or require extensive peripheral circuitry to modulate a synapse and are thus deficient in learning capability As a result they eliminate most of the density advantages gained by the adoption of nanoscale devices and fail to realize a functional computing system This

dissertation describes novel hardware architectures and neuron circuit designs that synergistically assemble the fundamental and significant elements for brain inspired computing Versatile CMOS spiking neurons that combine integrate and fire passive dense RRAM synapses drive capability dynamic biasing for adaptive power consumption in situ spike timing dependent plasticity STDP and competitive learning in compact integrated circuit modules are presented Real world pattern learning and recognition tasks using the proposed architecture were demonstrated with circuit level simulations A test chip was implemented and fabricated to verify the proposed CMOS neuron and hardware architecture and the subsequent chip measurement results successfully proved the idea The work described in this dissertation realizes a key building block for large scale integration of spiking neural network hardware and then serves as a step stone for the building of next generation energy efficient brain inspired cognitive computing systems Boise State University ScholarWorks   <u>Neuromorphic Computing Systems for Industry 4.0</u> Dhanasekar, S.,Sagayam, K. Martin,Vijh, Surbhi,Tyagi, Vipin,Norta, Alex,2023-07-19 As artificial intelligence AI processing moves from the cloud to the edge of the network battery powered and deeply embedded devices are challenged to perform AI functions such as computer vision and voice recognition Microchip Technology Inc via its Silicon Storage Technology SST subsidiary is addressing this challenge by significantly reducing power with its analog memory technology the memBrain Memory Solution The memBrain solution is being adopted by today s companies looking to advance machine learning capacities in edge devices Due to its ability to significantly reduce power this analog in memory computer solution is ideal for an AI application Neuromorphic Computing Systems for Industry 4 0 covers the available literature in the field of neural computing based microchip technology It provides further research opportunities in this dynamic field Covering topics such as emotion recognition biometric authentication and neural network protection this premier reference source is an essential resource for technology developers computer scientists engineers students and educators of higher education librarians researchers and academicians   **Hardware-Software Co-design for Neuromorphic Computing** Adarsha Balaji,2022 Neuromorphic devices represent an attempt to mimic the computational dynamics and distributed architecture of mammalian brains Mixed signal neuromorphic platforms executing Spiking Neural Networks SNNs show significant gains in computational speed and energy consumption when compared to recent deep learning accelerators However with growing model size and complexity of SNN based applications and learning algorithms allocating resources efficiently on neuromorphic hardware while ensuring optimal performance in terms of algorithm accuracy latency and energy consumption is becoming increasingly challenging Therefore there is a growing need for an extensible simulation framework that can 1 perform architectural explorations with SNNs including both platform based design of today s hardware and 2 hardware software co design and design technology co optimization of the future In this thesis a hardware software co design framework is presented with an aim to 1 design large scale SNNs 2 compile SNN based applications for neuromorphic hardware 3 optimize the allocation of resources on the neuromorphic platform to execute the

compiled SNN based application and 4 design a novel communication architecture CA for future neuromorphic platforms with an aim to address and ensure the scalability of crossbar based platforms The proposed framework will significantly improve the performance of existing neuromorphic platforms in terms of algorithm accuracy latency energy consumption and reliability and explore architectural improvements to address the limitations of existing platforms **Multi-memristive Synaptic Architectures for Training Neural Networks** Irem Boybat Kara,2020 Mots cl s de l auteur In memory computing neuromorphic computing memristive device multi memristive synaptic architecture neural network training artificial neural network spiking neural network fully memristive training mixed precision training binary memristive device **Spiking Neural Networks for Simultaneous Localization and Mapping in Neuromorphic Hardware** Raphaela Kreiser,2021

Neuromorphic Systems Engineering Tor Sverre Lande,2007-08-26 Neuromorphic Systems Engineering Neural Networks in Silicon emphasizes three important aspects of this exciting new research field The term neuromorphic expresses relations to computational models found in biological neural systems which are used as inspiration for building large electronic systems in silicon By adequate engineering these silicon systems are made useful to mankind Neuromorphic Systems Engineering Neural Networks in Silicon provides the reader with a snapshot of neuromorphic engineering today It is organized into five parts viewing state of the art developments within neuromorphic engineering from different perspectives Neuromorphic Systems Engineering Neural Networks in Silicon provides the first collection of neuromorphic systems descriptions with firm foundations in silicon Topics presented include large scale analog systems in silicon neuromorphic silicon auditory ear and vision eye systems in silicon learning and adaptation in silicon merging biology and technology micropower analog circuit design analog memory analog interchipcommunication on digital buses LIST Neuromorphic Systems Engineering Neural Networks in Silicon serves as an excellent resource for scientists researchers and engineers in this emerging field and may also be used as a text for advanced courses on the subject **Emulation of Bursting Neurons in Neuromorphic Hardware Based on Phase-Change Materials** Richard Meyes,2015 Intro CHAPTER 1 Introduction CHAPTER 2 A Biological Background 2 1 The Neuron 2 2 The Synapse 2 3 An Overall View CHAPTER 3 Experimental Emulations 3 1 Modeling STP and LTP in a CMOS Spiking NeuralNetwork Chip 3 2 Implementation of STDP based on Phase ChangeMaterial Synapses 3 3 Phase Change Materials for Artificial NeuralNetworks 3 4 An Overall View CHAPTER 4 Bursting Neurons 4 1 Physiological Mechanisms of Bursting 4 2 Bursts as a Unit of Neuronal Information 4 3 Bursting for Selective Communication 4 4 Modeling Neuronal Bursting Activity 4 5 An Overall View CHAPTER 5 A PCM Bursting Neuron 5 1 Voltage Controlled Relaxation Oscillation in a PCMDevice 5 2 The Analogy to Hippocampal Pyramidal BurstingNeurons 5 3 Simulation of a PCM Bursting Neuron 5 4 An Overall View CHAPTER 6 An Outlook on the Future APPENDIX A Quantification of the MembranePotential APPENDIX B Vocabulary List of Figures List of Tables Bibliography Acknowledgement **Dynamical Systems in Spiking Neuromorphic Hardware** Aaron Russell Voelker,2019 Dynamical

systems are universal computers They can perceive stimuli remember learn from feedback plan sequences of actions and coordinate complex behavioural responses The Neural Engineering Framework NEF provides a general recipe to formulate models of such systems as coupled sets of nonlinear differential equations and compile them onto recurrently connected spiking neural networks akin to a programming language for spiking models of computation The Nengo software ecosystem supports the NEF and compiles such models onto neuromorphic hardware In this thesis we analyze the theory driving the success of the NEF and expose several core principles underpinning its correctness scalability completeness robustness and extensibility We also derive novel theoretical extensions to the framework that enable it to far more effectively leverage a wide variety of dynamics in digital hardware and to exploit the device level physics in analog hardware At the same time we propose a novel set of spiking algorithms that recruit an optimal nonlinear encoding of time which we call the Delay Network DN Backpropagation across stacked layers of DNs dramatically outperforms stacked Long Short Term Memory LSTM networks a state of the art deep recurrent architecture in accuracy and training time on a continuous time memory task and a chaotic time series prediction benchmark The basic component of this network is shown to function on state of the art spiking neuromorphic hardware including Braindrop and Loihi This implementation approaches the energy efficiency of the human brain in the former case and the precision of conventional computation in the latter case   Efficient Methods and Architectures for Deep Neural Network Sequence Models Emmanuel Kahembwe Mbabazi,2021   **Energy Efficient Hardware Architectures for Memory Prohibitive Deep Neural Networks** Suhas Shivapakash,2024

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