

ARM Instruction Set Format

31	28:27	16:15	8:7	0					
Cond	0 0 1	Opcode	S	Rn	Rd	Operand2			
Cond	0 0 0 0 0 0	A S	Rd	Rn	Rs	1 0 0 1	Rm		
Cond	0 0 0 0 1	U A S	RdHi	RdLo	Rs	1 0 0 1	Rm		
Cond	0 0 0 1 0	B 0 0	Rn	Rd	0 0 0 0	1 0 0 1	Rm		
Cond	0 1 1	P U B W L	Rn	Rd	Offset				
Cond	1 0 0	P U S W L	Rn	Register List					
Cond	0 0 0	P U 1 W L	Rn	Rd	Offset1	1 S H 1	Offset2		
Cond	0 0 0	P U 0 W L	Rn	Rd	0 0 0 0	1 S H 1	Rm		
Cond	1 0 1 1	Offset							
Cond	0 0 0 1	0 0 1 0	1 1 1 1	1 1 1 1	1 1 1 1	0 0 0 1	Rn		
Cond	1 1 0	P U N W L	Rn	CRd	CPNum	Offset			
Cond	1 1 1 0	Op1		CRn	CRd	CPNum	Op2	0	CRm
Cond	1 1 1 0	Op1	L	CRn	Rd	CPNum	Op2	1	CRm
Cond	1 1 1 1	SWI Number							

Instruction type

Data processing / PSR Transfer

Multiply

Long Multiply (v3M / v4 only)

Swap

Load/Store Byte/Word

Load/Store Multiple

Halfword transfer: Immediate offset (v4 only)

Halfword transfer: Register offset (v4 only)

Branch

Branch Exchange (v4T only)

Coprocessor data transfer

Coprocessor data operation

Coprocessor register transfer

Software interrupt

Arm Instruction Set Assembly Language Utk

L Towne



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web goal 1 engage our learners through innovative teaching and learning practices enhance support for students with specific needs support the implementation of the curriculum enhance assessment and reporting strategies to support teaching and learning

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goal 1 improve student learning outcomes target 1 1 by 2022 for 75 of year 5 7 and 9 students to meet their learning goals in their individual learning plan each year in 2018 38 of year 5 7 and 9 students met their

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