4-Channel, Simultaneous Sampling, High Speed, 12-Bit ADC

AD7864

FEATURES

High speed (1.65 µs) 12-bit ADC
4 simultaneously sampled inputs
4 track-and-hold amplifiers
  0.35 µs track-and-hold acquisition time
  1.65 µs conversion time per channel
HW/SW select of channel sequence for conversion
Single-supply operation
Selection of input ranges
  ±10 V, ±5 V for AD7864-1
  ±2.5 V for AD7864-3 0 V to 2.5 V, 0 V to 5 V for AD7864-2
High speed parallel interface that allows interfacing to 3 V processors
Low power, 90 mW typical
Power saving mode, 20 µW typical
Overvoltage protection on analog inputs

APPLICATIONS

AC motor control
Uninterrupted power supplies
Data acquisition systems
Communications

GENERAL DESCRIPTION

The AD7864 is a high speed, low power, 4-channel, simultaneous sampling 12-bit analog-to-digital converter (ADC) that operates from a single 5 V supply. The part contains a 1.65 µs successive approximation ADC, four track-and-hold amplifiers, a 2.5 V reference, an on-chip clock oscillator, signal conditioning circuitry, and a high speed parallel interface. The input signals on four channels sample simultaneously preserving the relative phase information of the signals on the four analog inputs. The part accepts analog input ranges of ±10 V, ±5 V (AD7864-1), 0 V to +2.5 V, 0 V to +5 V (AD7864-2), and ±2.5 V (AD7864-3).

Any subset of the four channels can be converted to maximize the throughput rate on the selected sequence. Select the channels to convert via hardware (channel select input pins) or software (programming the channel select register).

A single conversion start signal ($\overline{CONVST}$) simultaneously places all the track-and-holds into hold and initiates a conversion sequence for the selected channels. The $\overline{EOC}$ signal indicates the end of each individual conversion in the selected conversion sequence. The BUSY signal indicates the end of the conversion sequence.

FUNCTIONAL BLOCK DIAGRAM

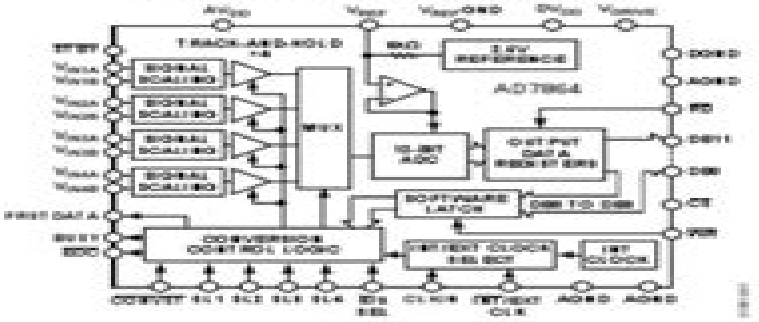

Figure 1.

Data is read from the part by a 12-bit parallel data bus using the standard $\overline{CS}$ and $\overline{RD}$ signals. Maximum throughput for a single channel is 500 kSPS. For all four channels, the maximum throughput is 130 kSPS for the read-during-conversion sequence operation. The throughput rate for the read-after-conversion sequence operation depends on the read cycle time of the processor. See the Timing and Control section. The AD7864 is available in a small (0.3 square inch area) 44-lead MQFP.

PRODUCT HIGHLIGHTS

1. Four track-and-hold amplifiers and a fast (1.65 µs) ADC for simultaneous sampling and conversion of any subset of the four channels.
2. A single 5 V supply consuming only 90 mW typical, makes it ideal for low power and portable applications. See the Standby Mode Operation section.
3. High speed parallel interface for easy connection to microprocessors, microcontrollers, and digital signal processors.
4. Available in three versions with different analog input ranges. The AD7864-1 offers the standard industrial input ranges of ±10 V and ±5 V; the AD7864-3 offers the common signal processing input range of ±2.5 V; the AD7864-2 can be used in unipolar, 0 V to 2.5 V and 0 V to 5 V, applications.
5. Features very tight aperture delay matching between the four input sample-and-hold amplifiers.

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4 Channel Simultaneous Sampling High Speed 12 Bit Adc

JR Anderson

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