



# Linux Programming By Example The Fundamentals

**Y Pai**



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web nov 7 2016 ds90003159b page 2 2017 microchip technology inc i<sup>2</sup>c protocol overview the i<sup>2</sup>c module follows the phillips i<sup>2</sup>c specification the module provides a bidirectional master slave synchronous interface between the pic microcontroller and other i<sup>2</sup>c supported devices these devices are connected via a two wire serial bus

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web the master synchronous serial port mssp is an integrated serial communications module the mssp contains two sub modules spi serial peripheral interface i<sup>2</sup>c inter integrated circuit the inter integrated circuit commonly referred to as i<sup>2</sup>c is a synchronous two wire bidirectional serial communications bus

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web jun 23 2016 key features of the i<sup>2</sup>c module include the following independent master and slave logic multi master support which prevents message losses in arbitration detects 7 bit and 10 bit device addresses with configurable address masking in slave mode detects general call addresses as defined in the i<sup>2</sup>c protocol automatic sclx clock

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web the i<sup>2</sup>c bus is a multi master serial data communication bus microcontrollers communicate in a master slave environment where the master devices initiate the communication and the devices are selected through addressing i<sup>2</sup>c operates with one or more master devices and one or more slave devices

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subsidiaries include `asf.h` define `data_length 10` packet data referenced by main and setup dma descriptor define slave address `0x12` referenced by main define `timeout 1000`

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