

Defect Detection with Transient Current Testing and its Potential for Deep Sub-micron CMOS ICs

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Abstract

Transient current testing (I_{DDT}) has been often cited as an alternative and/or supplement to I_{DDQ} testing. In this article we investigate the potential of transient current testing in faulty chip detection with silicon devices. The effectiveness of the I_{DDT} test method is compared with I_{DDQ} as well as with Sb -based voltage testing. Photon emission microscopy is used to localize defects in several faulty devices. Furthermore, the potential of I_{DDT} testing for leaky deep sub-micron devices is investigated.

1 Introduction

Quiescent current testing (I_{DDQ}) is an important ingredient of the test suite for digital VLSI. The contributions of I_{DDQ} testing in quality improvement, test cost reduction, burn-in elimination have been well recognized [1]. However, the effectiveness of conventional I_{DDQ} testing in deep sub-microns is expected to be eroded owing to the increased sub-threshold current in MOS transistors [2-5]. Many solutions have been proposed to contain the increased sub-threshold leakage and are documented elsewhere [3,5,6]. These solutions include utilization of reverse biasing techniques to reduce the sub-threshold leakage in the test mode [3,5], utilization of Silicon On Insulator (SOI) technology for a steeper sub-threshold swing [7,8], or utilization of multi-threshold transistors to contain the sub-threshold leakage [9]. Moreover, containment of sub-threshold leakage is an important parameter for low power and device reliability consideration. Therefore, many low power circuit-level techniques have been devised to significantly reduce the sub-threshold leakage current.

Typically these solutions require non-trivial changes in the standard cell library or in the process. In many applications such as high performance VLSI, these solutions may pose several restrictions. CMOS processes for such devices are aggressively scaled (V_T and gate oxide) and optimized for switching speed. As a result, these devices are not I_{DDQ} testable. Therefore, ensuring gate oxide quality and reliability is becoming an increasingly difficult as well as an expensive task.

In this article, we investigate the potential of transient current testing (I_{DDT}) as an alternative/supplement to I_{DDQ} testing. The motivation of this research comes from the following reasons: (i) To compare the effectiveness of I_{DDT} with respect to I_{DDQ} and voltage testing. For a production test method, the reproducibility of the test method is of prime importance. (ii) To investigate the feasibility of I_{DDT} based test techniques in a deep sub-micron environment. Current-based test techniques are much more sensitive compared to voltage-based counter parts. Owing to several factors, in deep sub-micron voltage-based test strategies are unlikely to guarantee quality expectations. (iii) To investigate the speed-up factor. For I_{DDQ} measurements, one does not have to wait till the current has reached the quiescent level. Hence, it is possible to enhance speed of the measurements. In other words, it is possible to perform I_{DDT} measurements at a significantly higher rate compared to I_{DDQ} measurements.

2 Previous Work

Some of the initial work on I_{DDT} was done by Frenzel and Marinus [10]. They simulated a small TTL circuit (few logic gates) assigning different sinusoidal waveforms on the inputs. They described complete power supply current as a signature of the Device Under Test (DUT). The signature of the DUT was compared with that of a golden device. In this manner a pass/fail criterion was established. So and Misaki [11] applied dynamic current monitoring techniques on SRAMs. To improve the defect detection capabilities of the dynamic current, they incorporated an extensive DFT strategy. The DFT scheme included separate V_{DD} and V_{SS} supplies for transient measurements, distributed switches to switch between the normal V_{DD} (V_{DD}), and a test V_{DD} (V_{SS}) only for dynamic current measurements. Furthermore, two dynamic current monitors and a set of controls are needed on the DUT. In their subsequent paper [12], the authors implemented the concept in silicon. The results reported showed that I_{DDT} is a better test method compared to I_{DDQ} and logic testing for open defects. However, the DFT implementation required is non-trivial and has implications for performance and test overhead.

Musipacific et al. [13] proposed the concept of Transient

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Interconnection Noise in VLSI Circuits Francesc Moll, Miquel Roca, 2004 Later simple models of crosstalk and switching noise are used to give an intuitive understanding of these problems Finally some verification and test issues related to interconnection noise are discussed Throughout the book the examples used to illustrate the discussion are based on digital CMOS circuits but the general treatment of the problems is from a fundamental point of view so that the discussion can be applied to different technologies

Microelectronics Failure Analysis, 2004-01-01 For newcomers cast into the waters to sink or swim as well as seasoned professionals who want authoritative guidance desk side this hefty volume updates the previous 1999 edition It contains the work of expert contributors who rallied to the job in response to a committee s call for help the committee was assigned to the update by the Electron

IEEE VLSI Test Symposium, 2005 **CMOS Electronics** Jaume Segura, Charles F. Hawkins, 2004-03-26 CMOS manufacturing environments are surrounded with symptoms that can indicate serious test design or reliability problems which in turn can affect the financial as well as the engineering bottom line This book educates readers including non engineers involved in CMOS manufacture to identify and remedy these causes This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test reliability failure analysis yield quality issues and problems Designed specifically for the many non electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities this is a practical guide to how CMOS electronics work how failures occur and how to diagnose and avoid them Key features Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure Unique descriptions of circuit failure mechanisms some found previously only in research papers and others new to this publication Targeted to the CMOS industry or students headed there and not a generic introduction to the broader field of electronics Examples exercises and problems are provided to support the self instruction of the reader

Proceedings of the ... International Conference on Microelectronics, 2002 **18th IEEE VLSI Test Symposium**, 2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test compaction and design validation analog BIST and functional test and verification issues Also covered are STIL extension IDDQ test and on line testing and fault tolerance Lacks a subject index Annotation copyrighted by Book News Inc Portland OR

19th IEEE VLSI Test Symposium, 2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are

gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc

Contactless VLSI Measurement and Testing Techniques Selahattin Sayil, 2017-11-16 This book provides readers with a comprehensive overview of the state of the art in optical contactless probing approaches in order to fill a gap in the literature on VLSI Testing The author highlights the inherent difficulties encountered with the mechanical probe and testability design approaches for functional and internal fault testing and shows how contactless testing might resolve many of the challenges associated with conventional mechanical wafer testing The techniques described in this book address the increasing demands for internal access of the logic state of a node within a chip under test

IC Test Using the Energy Consumption Ratio Wanli Jiang, 2000 **Conference Proceedings**, 2001 **Proceedings** Ieee, 2004 The proceedings of the 21st IEEE VLSI test symposium VTS 2003 describing innovations in the testing of integrated circuits and systems

Microelectronic Failure Analysis Richard J. Ross, Christian Boit, Donald Staab, 1999 Forty seven papers on electronics failure analysis provide an overview for newcomers to the field and a reference tool for the experienced analyst Topics include electron ion beam based techniques deprocessing and sample preparation and physical chemical defect characterization For the fourth ed *Proceedings*, 2002 **IDDQ Testing of VLSI Circuits** Ravi K. Gulati, Charles F. Hawkins, 2012-12-06 Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid 1970s Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs At that time this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current IDDQ contained defects Later this intuition was supported by data and analysis in the 1980s by Levi RACD Malaiya and Su SUNY Binghamton Soden and Hawkins Sandia Labs and the University of New Mexico Jacomino and co workers Laboratoire d Automatique de Grenoble and Maly and co workers Carnegie Mellon University Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs This is done for all or most nodes of the circuit For sequential circuits in particular the complexity of finding suitable tests is very high In comparison the IDDQ test does not observe the logic states but measures the integrated current that leaks through all gates In other words it is like measuring a patient s temperature to determine the state of health Despite perceived advantages during the years that followed its initial announcements skepticism about the practicality of IDDQ

testing prevailed The idea however provided a great opportunity to researchers New results on test generation fault simulation design for testability built in self test and diagnosis for this style of testing have since been reported After a decade of research we are definitely closer to practice *ISCAS 2001* ,2001 **Test Cost Reduction Techniques** Xiaoyun Sun,2005 On-Line Testing for VLSI Michael Nicolaidis,Yervant Zorian,Dhiraj Pradhan,2013-03-09 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Proceedings, International Test Conference 1996** ,1996 ITC is the World s largest premier technical conference on the testing and total quality of integrated electronics and the assemblies and systems that are based on them **Material Science, Engineering Research, Management and Information Technologies** Helen Zhang,David Jin,X.J. Zhao,2014-06-23 Selected peer reviewed papers from the 2014 4th International Conference on Engineering Materials Energy Management and Control MEMC 2014 June 21 22 2014 Wuhan China Asian Test Symposium ,2004

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