Sar Adc Matlab Code

M Carnoy

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    Emerging VLSI Devices, Circuits and Architectures Anu Gupta,Jai Gopal Pandey,Nitin Chaturvedi,Devesh Dwivedi,2024-10-18 This book constitutes the proceedings of the 27th International Symposium on VLSI Design and Test VDAT 2023 The 32 regular papers and 16 short papers presented in this book are carefully reviewed and selected from 220 submissions They are organized in topical sections as follows Low Power Integrated Circuits and Devices FPGA Based Design and Embedded Systems Memory Computing and Processor Design CAD for VLSI Emerging Integrated Circuits and Systems VLSI Testing and Security and System Level Design *Radiation Tolerant Nyquist Analog to Digital Converters* Zheyi Li,Laurent Berti,Paul Leroux,2025-09-30 This book presents the detailed design considerations and techniques for radiation tolerant RT Nyquist analog to digital converters ADC It begins with the fundamental radiation effects in space and its consequences in modern CMOS technology Next radiation effects on ADCs from the transistor level to the architectural level are examined and a detailed design tradeoffs and strategies for radiation tolerant ADCs are described The theory and hardening techniques are supported by measurement data from a high performance RT ADC prototype chip Two important flows which are a technology evaluation flow and an RT IC design flow are also covered in order to give a complete overview on how to achieve an effective RT circuits design **Ultra-Low-Voltage Frequency Synthesizer and Successive-Approximation Analog-to-Digital Converter for Biomedical Applications** Chung-Chih Hung,Shih-Hsing Wang,2021-12-07 This book introduces the origin of biomedical signals and the operating principles behind them and introduces the characteristics of common biomedical signals for subsequent signal measurement and judgment Since biomedical signals are captured by wearable devices sensor devices or implanted devices these devices are all battery powered to maintain long working time We hope to reduce their power consumption to extend service life especially for implantable devices because battery replacement can only be done through surgery Therefore we must understand how to design low power integrated circuits Both implantable and in vitro medical signal detectors require two basic components to collect and transmit biomedical signals an analog to digital converter and a frequency synthesizer because these measured biomedical signals are wirelessly transmitted to the relevant receiving unit The core unit of wireless transmission is the frequency synthesizer which provides a wide frequency range and stable frequency to demonstrate the quality and performance of the wireless transmitter Therefore the basic operating principle and model of the frequency synthesizer are introduced We also show design examples and measurement results of a low power low voltage integer N frequency synthesizer for biomedical applications The detection of biomedical signals needs to be converted into digital signals by an analog to digital converter to facilitate subsequent signal processing and recognition Therefore the operating principle of the analog to digital converter is introduced We also show implementation examples and measurement results of low power low voltage analog to digital converters for biomedical applications Proceedings of the 2nd International Conference on

Intelligent Technologies and Engineering Systems (ICITES2013) Jengnan Juang,Cheng-Yi Chen,Cheng-Fu Yang,2014-04-18 This book includes the original peer reviewed research papers from the conference Proceedings of the 2nd International Conference on Intelligent Technologies and Engineering Systems ICITES2013 which took place on December 12 14 2013 at Cheng Shiu University in Kaohsiung Taiwan Topics covered include laser technology wireless and mobile networking lean and agile manufacturing speech processing microwave dielectrics intelligent circuits and systems 3D graphics communications and structure dynamics and control   *Airborne Circularly Polarized SAR* Josaphat Tetuko Sri Sumantyo,Ming Yam Chua,Cahya Edi Santosa,Yuta Izumi,2023-04-25 A comprehensive resource on airborne synthetic aperture radar SAR systems Airborne Circularly Polarized SAR explains the theory system design hardware and software and applications of airborne circularly polarized SAR in environmental monitoring and other uses Readers learn how to build the hardware and software of circularly polarized SAR the antenna system and how to generate point target responses and images using the range doppler algorithm RDA from raw signal data The book discusses applications and analyzing techniques using a circularly polarized SAR system and image processing Images and MATLAB codes are provided to help professionals and researchers with their applications and future studies Features Provides the theory of circularly polarized wave and polarimetry related to system design scattering analysis polarimetric SAR and applications in microwave remote sensing Explains the real radio frequency RF system and the original antenna including circuit explanation and know how of measurement technique to adjust to the required parameter in system design Discusses the technique of ground test and flight mission to calibrate and validate the performance of airborne circularly polarized SAR Highlights image signal processing with MATLAB codes and how to obtain a single look complex SLC image for further applications Includes several applications of airborne circularly polarized SAR from international leading experts This book is beneficial to professionals researchers academics and graduate students from disciplines such as Electronic Engineering Radar Systems Aerospace Engineering Signal Processing Image Processing Environmental Remote Sensing   Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers Kofi A. A. Makinwa,Andrea Baschirotto,Pieter Harpe,2019-01-28 This book is based on the 18 invited tutorials presented during the 27th workshop on Advances in Analog Circuit Design Expert designers from both industry and academia present readers with information about a variety of topics at the frontiers of analog circuit design including the design of analog circuits in power constrained applications CMOS compatible sensors for mobile devices and energy efficient amplifiers and drivers For anyone involved in the design of analog circuits this book will serve as a valuable guide to the current state of the art Provides a state of the art reference in analog circuit design written by experts from industry and academia Presents material in a tutorial based format Covers the design of analog circuits in power constrained applications CMOS compatible sensors for mobile devices and energy efficient amplifiers and drivers **High-Resolution and High-Speed Integrated CMOS AD Converters for Low-Power Applications** Weitao Li,Fule

Li,Zhihua Wang,2017-08-01 This book is a step by step tutorial on how to design a low power high resolution not less than 12 bit and high speed not less than 200 MSps integrated CMOS analog to digital AD converter to respond to the challenge from the rapid growth of IoT The discussion includes design techniques on both the system level and the circuit block level In the architecture level the power efficient pipelined AD converter the hybrid AD converter and the time interleaved AD converter are described In the circuit block level the reference voltage buffer the opamp the comparator and the calibration are presented Readers designing low power and high performance AD converters won t want to miss this invaluable reference Provides an in depth introduction to the newest design techniques for the power efficient high resolution not less than 12 bit and high speed not less than 200 MSps AD converter Presents three types of power efficient architectures of the high resolution and high speed AD converter Discusses the relevant circuit blocks i e the reference voltage buffer the opamp and the comparator in two aspects relaxing the requirements and improving the performance   Proceedings of the ... IEEE Instrumentation and Measurement Technology Conference ,2004   **IEEE International Geoscience and Remote Sensing Symposium Proceedings** ,2001   **2003 IEEE Nuclear Science Symposium** ,2004   *IGARSS.* ,1981   Conference Proceedings ,2001   **Index to IEEE Publications** Institute of Electrical and Electronics Engineers,1998 Issues for 1973 cover the entire IEEE technical literature   **Science Abstracts** ,1995   *Charge-Sharing SAR ADCs for Low-Voltage Low-Power Applications* Taimur Rabuske,Jorge Fernandes,2016-08-02 This book introduces readers to the potential of charge sharing CS successive approximation register SAR analog to digital converters ADCs while providing extensive analysis of the factors that limit the performance of the CS topology The authors present guidelines and useful techniques for mitigating the limitations of the architecture while focusing on the implementation under restricted power budgets and voltage supplies   Adiabatic Charging in SAR ADCs Aleksandr Gusev,2024 Successive Approximation Register SAR is an established and well rounded Analog to Digital Converter ADC architecture allowing for medium resolution and medium conversion speed while being energy efficient and relatively small in area Switched capacitor Digital to Analog Converter DAC being an essential component of the SAR architecture in certain design configurations might contribute significantly to the overall ADC power consumption Adiabatic capacitor charging is a method that allows for increasing the charging efficiency using linear voltage or constant current to charge a capacitor A variation of this approach uses a series of small voltage steps instead of a voltage ramp which is particularly suitable for switched capacitor circuits as it does not require analog circuitry such as a voltage ramp generator or a current source This work investigates the stepwise capacitor charging approach applied to DAC in SAR ADC in terms of the architectural modifications and their influence on the resulting efficiency improvement The study begins with an estimation of the stepwise charging applied to a conventional DAC switching scheme The average energy consumption is derived as a function of the number of charging steps and resolution the results are verified in MATLAB For the implementation of the approach other switching schemes were considered the

selected monotonic switching scheme was then also modelled in MATLAB to evaluate the efficiency improvement depending on the number of charging steps in that case Stepwise charging requires several intermediate voltage levels in addition to the regular reference voltage The work includes the discussion and implementation of the onboard DC DC converter and the MATLAB model includes its influence on energy savings allowing for a design optimization as well as the selection of the converter s configuration in regards to the number of charging steps resolution and DAC unit capacitor size Finally the work describes a fabricated IC with two proof of concept ADC prototypes featuring 4 step charging applied to a 10 bit monotonic SAR ADC The circuits differ in terms of the DAC capacitance and conversion speed The first prototype has a sampling rate of 165 kS s and achieves SNDR of 57 63 dB The second prototype has a sampling rate of 1 MS s and achieves SNDR of 56 52 dB The architecture is designed with separated circuits for the SAR register and adiabatic charging control logic in order to better differentiate the control logic penalty related to stepwise charging To further identify the power savings in both prototypes the 1 step versions of each prototype with adiabatic circuitry removed from the layout are simulated in CAD and compared to the 4 step counterparts The evaluation of the first prototype shows a 26% reduction of the DAC power consumption including all the extra circuitry whereas the second prototype establishes the limitation of the approach where the energy savings were overpowered by the control logic penalty and DC DC converter switching losses The work discusses this limitation in detail describing the applicability area of adiabatic charging The proposed method allows the inclusion of these types of losses to optimize the configuration and estimate the benefits of the adiabatic switching in each case

Strategies for Reduced-code Static Testing of SAR ADCs Renato Silveira Feitoza,2021 Characterizing the static linearity performance is one of the key tasks in the test of an Analog to Digital converter ADC Normally the static linearity performance figures are measured during the production phase and the standard methodologies in the industry require the collection of a large amount of data since each code needs to be measured a few times to average the effect of noise Reduced code techniques for ADC static linearity test have the potential to drastically reduce the number of necessary measurements for a complete static linearity characterization These techniques take advantage of the repetitive operation of certain families of converters such as pipeline successive approximation registers SARs cyclic etc In this thesis novel reduced code techniques for static linearity test of SAR ADCs are presented They are based on the on chip generation and measurement of the transitions of the internal digital to analog converter DAC of the ADC This allows inferring the complete transfer function of the ADC by measuring only a carefully selected subset of the total set of codes greatly reducing the global test time Moreover the inherent simplification of static linearity tests provided by reduced code techniques may open the door to a full built in self test BIST implementation This way tester requirements can be relaxed and test cost may be further contained by moving static linearity test resources to the device under test itself The proposed test methodology does not require a test stimulus and it is shown that the necessary measurements can be easily extracted by reconfiguring portions of the SAR into a

low resolution incremental converter   *Synthetic Aperture Radar Signal Processing with MATLAB Algorithms* Mehrdad Soumekh,1999 An up to date analysis of the SAR wavefront reconstruction signal theory and its digital implementation With the advent of fast computing and digital information processing techniques synthetic aperture radar SAR technology has become both more powerful and more accurate Synthetic Aperture Radar Signal Processing with MATLAB Algorithms addresses these recent developments providing a complete up to date analysis of SAR and its associated digital signal processing algorithms This book introduces the wavefront reconstruction signal theory that underlies the best SAR imaging methods and provides clear guidelines to system design implementation and applications in diverse areas from airborne reconnaissance to topographic imaging of ocean floors to surveillance and air traffic control to medical imaging techniques and numerous others Enabling professionals in radar signal and image processing to use synthetic aperture technology to its fullest potential this work Includes M files to supplement this book that can be retrieved from The MathWorks anonymous FTP server at ftp ftp mathworks com pub books soumekh Provides practical examples and results from real SAR ISAR and CSAR databases Outlines unique properties of the SAR signal that cannot be found in other information processing systems Examines spotlight SAR stripmap SAR circular SAR and monopulse SAR modalities Discusses classical SAR processing issues such as motion compensation and radar calibration   *Modeling of Channel Mismatch in Time-interleaved SAR ADC*Project Supported by the National Natural Science Foundation of China (Nos. 61234002, 61322405, 61306044, 61376033) and the National High-Tech Program of China (No. 2013AA014103).* ,2015 Abstract In a time interleaved analog to digital converter TI ADC several individual ADCs operate in parallel to achieve a higher sampling rate Low power consumption as well as good linearity can be obtained by applying successive approximation register SAR converters as sub channel ADCs In spite of the advantages this structure suffers from three mismatches which are offset mismatch gain mismatch and time skew This paper focuses on a TI SAR ADC with a number of channels The mismatch effects in the frequency domain are analyzed and the derived close form formulas are verified based on Matlab In addition we clarify that the standard deviation of DNL and INL of an M channel TI ADC is reduced by a factor of M compared to a single channel ADC The formulas can be used to derive the corresponding requirements when designing a TI ADC Our analysis process is able to inform the study of calibration algorithms   An 11-bit 20MS/s SAR ADC Using a Low-complexity Code-dependent Reference Ripple Suppression Technique 马嘉泽,2019

Uncover the mysteries within Crafted by is enigmatic creation, **Sar Adc Matlab Code** . This downloadable ebook, shrouded in suspense, is available in a PDF format (PDF Size: *). Dive into a world of uncertainty and anticipation. Download now to unravel the secrets hidden within the pages.

Table of Contents Sar Adc Matlab Code

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