Automatic Parallelization
An Overview of Fundamental Compiler Techniques

Samuel P. Midkiff

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   Automatic Parallelization Samuel Midkiff,2022-06-01 Compiling for parallelism is a longstanding topic of compiler research This book describes the fundamental principles of compiling regular numerical programs for parallelism We begin with an explanation of analyses that allow a compiler to understand the interaction of data reads and writes in different statements and loop iterations during program execution These analyses include dependence analysis use def analysis and pointer analysis Next we describe how the results of these analyses are used to enable transformations that make loops more amenable to parallelization and discuss transformations that expose parallelism to target shared memory multicore and vector processors We then discuss some problems that arise when parallelizing programs for execution on distributed memory machines Finally we conclude with an overview of solving Diophantine equations and suggestions for further readings in the topics of this book to enable the interested reader to delve deeper into the field Table of Contents Introduction and overview Dependence analysis dependence graphs and alias analysis Program parallelization Transformations to modify and eliminate dependences Transformation of iterative and recursive constructs Compiling for distributed memory machines Solving Diophantine equations A guide to further reading   Parallel Processing, 1980 to 2020 Robert Kuhn,David Padua,2022-05-31 This historical survey of parallel processing from 1980 to 2020 is a follow up to the authors 1981 Tutorial on Parallel Processing which covered the state of the art in hardware programming languages and applications Here we cover the evolution of the field since 1980 in parallel computers ranging from the Cyber 205 to clusters now approaching an exaflop to multicore microprocessors and Graphic Processing Units GPUs in commodity personal devices parallel programming notations such as OpenMP MPI message passing and CUDA streaming notation and seven parallel applications such as finite element analysis and computer vision Some things that looked like they would be major trends in 1981 such as big Single Instruction Multiple Data arrays disappeared for some time but have been revived recently in deep neural network processors There are now major trends that did not exist in 1980 such as GPUs distributed memory machines and parallel processing in nearly every commodity device This book is intended for those that already have some knowledge of parallel processing today and want to learn about the history of the three areas In parallel hardware every major parallel architecture type from 1980 has scaled up in performance and scaled out into commodity microprocessors and GPUs so that every personal and embedded device is a parallel processor There has been a confluence of parallel architecture types into hybrid parallel systems Much of the impetus for change has been Moore s Law but as clock speed increases have stopped and feature size decreases have slowed down there has been increased demand on parallel processing to continue performance gains In programming notations and compilers we observe that the roots of today s programming notations existed before 1980 And that through a great deal of research the most widely used programming notations today although the result of much broadening of these roots remain close to target system architectures allowing the programmer to almost

explicitly use the target s parallelism to the best of their ability The parallel versions of applications directly or indirectly impact nearly everyone computer expert or not and parallelism has brought about major breakthroughs in numerous application areas Seven parallel applications are studied in this book **A Primer on Memory Persistency** Vaibhav Gogte,Aasheesh Kolli,Thomas F. Wenisch,2022-02-09 This book introduces readers to emerging persistent memory PM technologies that promise the performance of dynamic random access memory DRAM with the durability of traditional storage media such as hard disks and solid state drives SSDs Persistent memories PMs such as Intel s Optane DC persistent memories are commercially available today Unlike traditional storage devices PMs can be accessed over a byte addressable load store interface with access latency that is comparable to DRAM Unfortunately existing hardware and software systems are ill equipped to fully avail the potential of these byte addressable memory technologies as they have been designed to access traditional storage media over a block based interface Several mechanisms have been explored in the research literature over the past decade to design hardware and software systems that provide high performance access to PMs Because PMs are durable they can retain data across failures such as power failures and program crashes Upon a failure recovery mechanisms may inspect PM data reconstruct state and resume program execution Correct recovery of data requires that operations to the PM are properly ordered during normal program execution Memory persistency models define the order in which memory operations are performed at the PM Much like memory consistency models memory persistency models may be relaxed to improve application performance Several proposals have emerged recently to design memory persistency models for hardware and software systems and for high level programming languages These proposals differ in several key aspects they relax PM ordering constraints introduce varying programmability burden and introduce differing granularity of failure atomicity for PM operations This primer provides a detailed overview of the various classes of the memory persistency models their implementations in hardware programming languages and software systems proposed in the recent research literature and the PM ordering techniques employed by modern processors Data Orchestration in Deep Learning Accelerators Tushar Krishna,Hyoukjun Kwon,Angshuman Parashar,Michael Pellauer,Ananda Samajdar,2020-08-18 This Synthesis Lecture focuses on techniques for efficient data orchestration within DNN accelerators The End of Moore s Law coupled with the increasing growth in deep learning and other AI applications has led to the emergence of custom Deep Neural Network DNN accelerators for energy efficient inference on edge devices Modern DNNs have millions of hyper parameters and involve billions of computations this necessitates extensive data movement from memory to on chip processing engines It is well known that the cost of data movement today surpasses the cost of the actual computation therefore DNN accelerators require careful orchestration of data across on chip compute network and memory elements to minimize the number of accesses to external DRAM The book covers DNN dataflows data reuse buffer hierarchies networks on chip and automated design space exploration It concludes with data orchestration challenges with

compressed and sparse DNNs and future trends The target audience is students engineers and researchers interested in designing high performance and low energy accelerators for DNN inference **Deep Learning Systems** Andres Rodriguez,2022-05-31 This book describes deep learning systems the algorithms compilers and processor components to efficiently train and deploy deep learning models for commercial applications The exponential growth in computational power is slowing at a time when the amount of compute consumed by state of the art deep learning DL workloads is rapidly growing Model size serving latency and power constraints are a significant challenge in the deployment of DL models for many applications Therefore it is imperative to codesign algorithms compilers and hardware to accelerate advances in this field with holistic system level and algorithm solutions that improve performance power and efficiency Advancing DL systems generally involves three types of engineers 1 data scientists that utilize and develop DL algorithms in partnership with domain experts such as medical economic or climate scientists 2 hardware designers that develop specialized hardware to accelerate the components in the DL models and 3 performance and compiler engineers that optimize software to run more efficiently on a given hardware Hardware engineers should be aware of the characteristics and components of production and academic models likely to be adopted by industry to guide design decisions impacting future hardware Data scientists should be aware of deployment platform constraints when designing models Performance engineers should support optimizations across diverse models libraries and hardware targets The purpose of this book is to provide a solid understanding of 1 the design training and applications of DL algorithms in industry 2 the compiler techniques to map deep learning code to hardware targets and 3 the critical hardware features that accelerate DL systems This book aims to facilitate co innovation for the advancement of DL systems It is written for engineers working in one or more of these areas who seek to understand the entire system stack in order to bettercollaborate with engineers working in other parts of the system stack The book details advancements and adoption of DL models in industry explains the training and deployment process describes the essential hardware architectural features needed for today s and future models and details advances in DL compilers to efficiently execute algorithms across various hardware targets Unique in this book is the holistic exposition of the entire DL system stack the emphasis on commercial applications and the practical techniques to design models and accelerate their performance The author is fortunate to work with hardware software data scientist and research teams across many high technology companies with hyperscale data centers These companies employ many of the examples and methods provided throughout the book *The Datacenter as a Computer* Luiz André Barroso,Urs Hölzle,Parthasarathy Ranganathan,2018-10-29 This book describes warehouse scale computers WSCs the computing platforms that power cloud computing and all the great web services we use every day It discusses how these new systems treat the datacenter itself as one massive computer designed at warehouse scale with hardware and software working in concert to deliver good levels of internet service performance The book details the architecture of WSCs and covers the main factors influencing their design

operation and cost structure and the characteristics of their software base Each chapter contains multiple real world examples including detailed case studies and previously unpublished details of the infrastructure used to power Google s online services Targeted at the architects and programmers of today s WSCs this book provides a great foundation for those looking to innovate in this fascinating and important area but the material will also be broadly interesting to those who just want to understand the infrastructure powering the internet The third edition reflects four years of advancements since the previous edition and nearly doubles the number of pictures and figures New topics range from additional workloads like video streaming machine learning and public cloud to specialized silicon accelerators storage and network building blocks and a revised discussion of data center power and cooling and uptime Further discussions of emerging trends and opportunities ensure that this revised edition will remain an essential resource for educators and professionals working on the next generation of WSCs **Security Basics for Computer Architects** Ruby B. Lee,2013-09-01 Design for security is an essential aspect of the design of future computers However security is not well understood by the computer architecture community Many important security aspects have evolved over the last several decades in the cryptography operating systems and networking communities This book attempts to introduce the computer architecture student researcher or practitioner to the basic concepts of security and threat based design Past work in different security communities can inform our thinking and provide a rich set of technologies for building architectural support for security into all future computers and embedded computing devices and appliances I have tried to keep the book short which means that many interesting topics and applications could not be included What the book focuses on are the fundamental security concepts across different security communities that should be understood by any computer architect trying to design or evaluate security aware computer architectures *Hardware and Software Support for Virtualization* Edouard Bugnion,Jason Nieh,Dan Tsafrir,2017-02-21 This book focuses on the core question of the necessary architectural support provided by hardware to efficiently run virtual machines and of the corresponding design of the hypervisors that run them Virtualization is still possible when the instruction set architecture lacks such support but the hypervisor remains more complex and must rely on additional techniques Despite the focus on architectural support in current architectures some historical perspective is necessary to appropriately frame the problem The first half of the book provides the historical perspective of the theoretical framework developed four decades ago by Popek and Goldberg It also describes earlier systems that enabled virtualization despite the lack of architectural support in hardware As is often the case theory defines a necessary but not sufficient set of features and modern architectures are the result of the combination of the theoretical framework with insights derived from practical systems The second half of the book describes state of the art support for virtualization in both x86 64 and ARM processors This book includes an in depth description of the CPU memory and I O virtualization of these two processor architectures as well as case studies on the Linux KVM VMware and Xen hypervisors It concludes with a performance

comparison of virtualization on current generation x86 and ARM based systems across multiple hypervisors   <u>Quantum Computer Systems: Research for Noisy Intermediate-Scale Quantum Computers</u> Yongshan Ding,Frederic T. Chong,2020-06-17 This book targets computer scientists and engineers who are familiar with concepts in classical computer systems but are curious to learn the general architecture of quantum computing systems It gives a concise presentation of this new paradigm of computing from a computer systems point of view without assuming any background in quantum mechanics As such it is divided into two parts The first part of the book provides a gentle overview on the fundamental principles of the quantum theory and their implications for computing The second part is devoted to state of the art research in designing practical quantum programs building a scalable software systems stack and controlling quantum hardware components Most chapters end with a summary and an outlook for future directions This book celebrates the remarkable progress that scientists across disciplines have made in the past decades and reveals what roles computer scientists and engineers can play to enable practical scale quantum computing   *Conference Proceedings* ,2000   <u>Languages and Compilers for Parallel Computing</u> Samuel P. Midkiff,José E. Moreira,Manish Gupta,2014-01-15   *Compiling Programs with User Parallelism* Samuel P. Midkiff,David A. Padua,Ronald Kaplan Cytron,1989 Abstract The parallelization and analysis techniques used in today s optimizing compilers have been designed assuming that the source program is sequential When programs with user parallelism are to be parallelized standard data dependence tests are insufficient to ensure the legality of the transformations This paper describes an additional test that guarantees the legality of parallelizing transformations in programs with user parallelism expressed as cobegin statements The constraints revealed by the additional test are represented by adding additional dependences to the dependence graph allowing standard transformations to proceed normally   <u>A Study of Automatic Parallelization Techniques</u> Douglas W. Kelley,1994   **Compiler Algorithms for Synchronization** Samuel P. Midkiff,David A. Padua,1987   **Automatic Parallelization Techniques for Massively Parallel Machines** Alyson Laura Thring,1988   **Input/Output Intensive Massively Parallel Computing** Peter Brezany,1997-04-09 Massively parallel processing is currently the most promising answer to the quest for increased computer performance This has resulted in the development of new programming languages and programming environments and has stimulated the design and production of massively parallel supercomputers The efficiency of concurrent computation and input output essentially depends on the proper utilization of specific architectural features of the underlying hardware This book focuses on development of runtime systems supporting execution of parallel code and on supercompilers automatically parallelizing code written in a sequential language Fortran has been chosen for the presentation of the material because of its dominant role in high performance programming for scientific and engineering applications   **Automatic Generation of Synchronization Instructions for Parallel Processors** Samuel Pratt Midkiff,University of Illinois at Urbana-Champaign. Center for Supercomputing Research and Development,1986   **A Unifying Language**

Approach to Automatic Parallelization Howard Bowman,1992   Semantic-Aware Automatic Parallelization of Modern Applications Using High-Level Abstractions ,2009 Automatic introduction of OpenMP for sequential applications has attracted significant attention recently because of the proliferation of multicore processors and the simplicity of using OpenMP to express parallelism for shared memory systems However most previous research has only focused on C and Fortran applications operating on primitive data types Modern applications using high level abstractions such as C STL containers and complex user defined class types are largely ignored due to the lack of research compilers that are readily able to recognize high level object oriented abstractions and leverage their associated semantics In this paper we use a source to source compiler infrastructure ROSE to explore compiler techniques to recognize high level abstractions and to exploit their semantics for automatic parallelization Several representative parallelization candidate kernels are used to study semantic aware parallelization strategies for high level abstractions combined with extended compiler analyses Preliminary results have shown that semantics of abstractions can help extend the applicability of automatic parallelization to modern applications and expose more opportunities to take advantage of multicore processors   Automatic Parallelization Christoph W Kessler,2012-04-18

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