ANSYS

GPU Accelerator and co-processor Capabilities *
Release 18.2

* Used in support of the GPU to process certain calculations and less other computations for faster performance during a solution.
- Acceleration can be used for both shared memory parallel processing (shared memory, SMP), and distributed memory parallel processing (Distributed DMP).
- Acceleration is available for both Windows and Linux.

Support by Applications

ANSYS Mechanical APDL supports all NVIDIA Tesla series cards and the following Quadro series cards: K6000, K4000, K5200, K6000, K5000, GP100, P5000, P6000. Additionally, **ANSYS Mechanical APDL** supports the following Intel Xeon Phi co-processor cards: 31x1D, 5110 and 7120. When using the sparse solver or eigensolvers based on the sparse solver with NVIDIA cards, additional combinations apply (please consult the ANSYS installation guide for details).

ANSYS Fluent supports NVIDIA CUDA-enabled Tesla and Quadro series and tested and certain cards.

ANSYS PolyFlow supports all NVIDIA Tesla series cards and the following Quadro series cards: K6000, K4000, K5200, K5000, GP100, P5000, P6000.

ANSYS EMIT supports NVIDIA Tesla P series, Tesla K Series, Quadro M series, GeForce GTX Series and GeForce GT Series.

ANSYS HFSS supports NVIDIA Tesla P series, C20 Series, Tesla K Series, Quadro K Series (K5000 and above).

ANSYS ICEPAK supports NVIDIA CUDA-enabled Tesla and Quadro series and certain cards.

ANSYS Slwave supports NVIDIA Tesla P series, C20 Series, Tesla K Series, Quadro K Series (K5000 and above).

ANSYS Savant supports NVIDIA Tesla P series, Tesla K Series, Quadro M Series, GeForce GTX Series and GeForce GT Series.

Application	Manufacturer	Product Series	Card / GPU	Tested Platform	Tested Operating System Version
ANSYS Mechanical APDL	Intel	Xeon Phi	31x1D	Windows x64	Windows Server 2012
	NVIDIA		7120A	Linux x64	Red Hat 6.4
		Quadro	8 P100	Windows x64	Windows 7
		Tesla	C2070	Linux x64	Red Hat 6.4
			C2075	Windows 7	Windows 7
			M2075	Linux x64	Red Hat 6.4
ANSYS Fluent	NVIDIA	Quadro	8 P100	Linux x64	Red Hat 7.2
			K5000	Windows x64	Windows 7
		Tesla	C2075	Windows x64	Windows 10
			M60	Windows x64	Windows 10
				Linux x64	SUSE 12 (SP1)
			K80	Linux x64	Red Hat 7.2
			M2075	Windows x64	Windows 7
			P100	Linux x64	SUSE 12 (SP1)

Application	Manufacturer	Product Series	Card / GPU	Tested Platform	Tested Operating System Version
ANSYS PolyFlow	NVIDIA	Quadro	K2000	Linux x64	Red Hat 7.2 / SUSE 11 (SP3)
			K5000	Linux x64	Red Hat 6.4
			M4000	Linux x64	CentOS 7.0
			P6000 (Dual)	Windows x64	Windows 10
		Tesla	K20c	Windows x64	Windows 7
			K80	Linux x64	Red Hat 7.2
ANSYS EMIT	NVIDIA	Quadro	M4000	Windows x64	Windows 10
				Linux x64	SUSE 12 (SP1)
		Tesla	K20c	Windows x64	Windows 7
			K40c	Windows x64	Windows 7
			P100	Windows x64	Windows Server 2012 R2
		GeForce	GTX 970	Windows x64	Windows 8.1
ANSYS HFSS	NVIDIA	Quadro	8 P100	Windows x64	Windows 7
			K5000	Windows x64	Windows 7
		Tesla	C2075	Windows x64	Windows 7
			K20	Windows x64	Windows 7
			K20c	Windows x64	Windows 7
			K20m	Linux x64	Red Hat 6.7
			K40c	Windows x64	Windows 7
			K80	Windows x64	Windows 8.1
				Linux x64	Red Hat 6.7
			P100	Windows x64	Windows 8.1
ANSYS ICEPAK	NVIDIA	Quadro	K5000	Windows x64	Windows 7
			M4000	Windows x64	Windows 10
		Tesla	K80	Windows x64	Windows 8.1
				Linux x64	Red Hat 7.2
			M2075	Windows x64	Windows 7
			P100	Linux x64	SUSE 12 (SP1)

Gpu Accelerator And Co Processor Capabilities Ansys

Xuan Shi,Volodymyr Kindratenko,Chaowei Yang

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   Implementation and Performance Analysis of Many-body Quantum Chemical Methods on the Intel Xeon Phi Coprocessor and NVIDIA GPU Accelerator Bobo Shi,2016 The tensor contraction are performed using BLAS DGEMM on coprocessor accelerator Then the result is post processed using a 6 dimensional loop For Intel Xeon Phi implementation OpenMP is used to bind threads to physical processing units on Xeon Phi coprocessors The OpenMP threads affinity are tuned for Intel Xeon Phi Coprocessor to obtain best performance For GPU a algorithm is designed to map the 6 dimensional loop post processing to CUDA threads gridDim and blockDim are tuned to reach best performance 4x and 9x 13x overall speedup is obtained for Intel Xeon Phi and GPU implementation respectively   *Modern Accelerator Technologies for Geographic Information Science* Xuan Shi,Volodymyr Kindratenko,Chaowei Yang,2013-10-27 This book explores the impact of augmenting novel architectural designs with hardware based application accelerators The text covers comprehensive aspects of the applications in Geographic Information Science remote sensing and deploying Modern Accelerator Technologies MAT for geospatial simulations and spatiotemporal analytics MAT in GIS applications MAT in remotely sensed data processing and analysis heterogeneous processors many core and highly multi threaded processors and general purpose processors are also presented This book includes case studies and closes with a chapter on future trends Modern Accelerator Technologies for GIS is a reference book for practitioners and researchers working in geographical information systems and related fields Advanced level students in geography computational science computer science and engineering will also find this book useful   Coprocessor Acceleration for Domain-specific Computing Yi Zou,2012 There is a growing trend to use coprocessors to offload and accelerate domain specific applications in order to obtain significant performance improvement and energy power reductions Two important coprocessor components in the heterogeneous system are the GPU and FPGA GPU graphics processing unit is increasingly used as a data parallel coprocessor for general computations The newest GPU has a much larger number of cores compared to CPU and very high peak FLOPS FPGA field programmable gate array on the other hand allows users to customize at fine grain level the computational data path and memory hierarchy according to the exact need of the applications FPGA excels in integer operations and bit level operations The thesis starts with several coprocessor acceleration examples for our focus application domains the first domain is on VLSICAD algorithms and the second is on computational medical imaging We detail application acceleration examples in the domains including lithography simulation for IC manufacturing medical image reconstruction using compressive sensing and medical image registration using fluid models Both GPU accelerated versions and FPGA accelerated versions have been implemented Based on these implementations we then analyze the performance and energy trade offs the interaction between the diverse application requirements and a spectrum of hardware systems and how those domain specific coprocessor acceleration case studies further bring us insights for domain specific architecture innovations In the end we showcase an example for

collaborative execution on the heterogeneous platform Different scheduling policies are needed to optimize performance or energy The thesis concludes as we present reusable architecture templates and realizations for futuristic accelerator rich CMPs

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