

Core Overview

The UART core with Avalon® interface implements a method to communicate serial character streams between an embedded system on an Altera® FPGA and an external device. The core implements the RS-232 protocol timing, and provides adjustable baud rate, parity, stop, and data bits, and optional RTS/CTS flow control signals. The feature set is configurable, allowing designers to implement just the necessary functionality for a given system.

The core provides an Avalon Memory-Mapped (Avalon-MM) slave interface that allows Avalon-MM master peripherals (such as a Nios® II processor) to communicate with the core simply by reading and writing control and data registers.

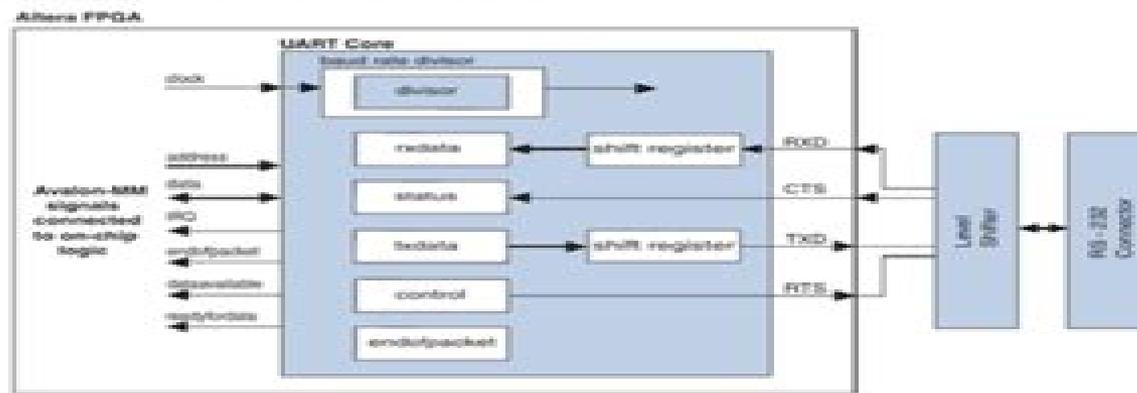
The UART core is SOPC Builder-ready and integrates easily into any SOPC Builder-generated system. This chapter contains the following sections:

- "Functional Description"
- "Device Support" on page 6-3
- "Instantiating the Core in SOPC Builder" on page 6-3
- "Simulation Considerations" on page 6-7
- "Software Programming Model" on page 6-8

Functional Description

Figure 6-1 shows a block diagram of the UART core.

Figure 6-1. Block Diagram of the UART Core in a Typical System



6 Uart Core Altera

Tobias Bleicker

A decorative red circular graphic with a gradient, positioned to the right of the author's name.

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Embedded SoPC Design with Nios II Processor and VHDL Examples Pong P. Chu, 2011-09-26 The book is divided into four major parts Part I covers HDL constructs and synthesis of basic digital circuits Part II provides an overview of embedded software development with the emphasis on low level I O access and drivers Part III demonstrates the design and development of hardware and software for several complex I O peripherals including PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides three case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology The book utilizes FPGA devices Nios II soft core processor and development platform from Altera Co which is one of the two main FPGA manufactures Altera has a generous university program that provides free software and discounted prototyping boards for educational institutions details at www.altera.com/university The two main educational prototyping boards are known as DE1 99 and DE2 269 All experiments can be implemented and tested with these boards A board combined with this book becomes a turn key solution for the SoPC design experiments and projects Most HDL and C codes in the book are device independent and can be adapted by other prototyping boards as long as a board has similar I O configuration

Architecture of Computing Systems Martin Schulz, Carsten Trinitis, Nikela Papadopoulou, Thilo Pionteck, 2022-12-13 This book constitutes the proceedings of the 35th International Conference on Architecture of Computing Systems ARCS 2022 held virtually in July 2022 The 18 full papers in this volume were carefully reviewed and selected from 35 submissions ARCS provides a platform covering newly emerging and cross cutting topics such as autonomous and ubiquitous systems reconfigurable computing and acceleration neural networks and artificial intelligence The selected papers cover a variety of topics from the ARCS core domains including energy efficiency applied machine learning hardware and software system security reliable and fault tolerant systems and organic computing

Embedded SoPC Design with Nios II Processor and Verilog Examples Pong P. Chu, 2012-05-14 Explores the unique hardware programmability of FPGA based embedded systems using a learn by doing approach to introduce the concepts and techniques for embedded SoPC design with Verilog An SoPC system on a programmable chip integrates a processor memory modules I O peripherals and custom hardware accelerators into a single FPGA field programmable gate array device In addition to the customized software customized hardware can be developed and incorporated into the embedded system as well allowing us to configure the soft core processor create tailored I O interfaces and develop specialized hardware accelerators for computation intensive tasks Utilizing an Altera FPGA prototyping board and its Nios II soft core processor *Embedded SoPC Design with Nios II Processor and Verilog Examples* takes a learn by doing approach to illustrate the hardware and software design and development process by including realistic projects that can be implemented and tested on the board Emphasizing hardware design and integration throughout the book is divided

into four major parts Part I covers HDL and synthesis of custom hardware Part II introduces the Nios II processor and provides an overview of embedded software development Part III demonstrates the design and development of hardware and software of several complex I O peripherals including a PS2 keyboard and mouse a graphic video controller an audio codec and an SD secure digital card Part IV provides several case studies of the integration of hardware accelerators including a custom GCD greatest common divisor circuit a Mandelbrot set fractal circuit and an audio synthesizer based on DDFS direct digital frequency synthesis methodology While designing and developing an embedded SoPC can be rewarding the learning can be a long and winding journey This book shows the trail ahead and guides readers through the initial steps to exploit the full potential of this emerging methodology

Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese,2007-11-14 A practical and fascinating book on a topic at the forefront of communications technology Field Programmable Gate Arrays FPGAs are on the verge of revolutionizing digital signal processing Novel FPGA families are replacing ASICs and PDSs for front end digital signal processing algorithms at an accelerating rate The efficient implementation of these algorithms is the main goal of this book It starts with an overview of today s FPGA technology devices and tools for designing state of the art DSP systems Each of the book s chapter contains exercises The VERILOG source code and a glossary are given in the appendices *EDN, Electrical Design News* ,2000 **Electronic Design** ,2002

12th International Workshop on Rapid System Prototyping IEEE Computer Society. Design Automation Technical Committee,2001 The proceedings from the June 2001 conference in Monterey California include 30 papers on hardware case studies reconfiguring computing communications systems distributed prototyping systems modeling model based prototyping efficient evaluation methodologies and tools Keynote addresses on **Radioengineering** ,2006 **Embedded Systems**

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