

4-bit Synchronous Counter (74LS161)

```
// 4-bit counter

module counter_4bit(clk, nclr, nload, ent, enp, rco, count, parallel_in) :

    input  clk ;
    input  nclr ;
    input  nload ;
    input  ent ;
    input  enp ;
    output rco ;
    output [3:0] count ;
    input  [3:0] parallel_in ;

    reg    [3:0] count ;
    reg    rco ;

    always @ (count or ent)
    if ((count == 15) && (ent == 1'b1))
        rco = 1'b1 ;
    else
        rco = 1'b0 ;

    always @ (posedge clk or negedge nclr)
    begin
        if (nclr == 1'b0)
            count <= 4'd0 ;
        else if (nload == 1'b0)
            count <= parallel_in ;
        else if ((ent == 1'b1) && (enp == 1'b1))
            count <= (count + 1) & 16 ;
    end
endmodule
```

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Jin-Ying Zhang



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Table of Contents 4 Bit Counter Verilog Code Davefc

1. Understanding the eBook 4 Bit Counter Verilog Code Davefc
 - The Rise of Digital Reading 4 Bit Counter Verilog Code Davefc
 - Advantages of eBooks Over Traditional Books
2. Identifying 4 Bit Counter Verilog Code Davefc
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an 4 Bit Counter Verilog Code Davefc
 - User-Friendly Interface

4. Exploring eBook Recommendations from 4 Bit Counter Verilog Code Davefc
 - Personalized Recommendations
 - 4 Bit Counter Verilog Code Davefc User Reviews and Ratings
 - 4 Bit Counter Verilog Code Davefc and Bestseller Lists
5. Accessing 4 Bit Counter Verilog Code Davefc Free and Paid eBooks
 - 4 Bit Counter Verilog Code Davefc Public Domain eBooks
 - 4 Bit Counter Verilog Code Davefc eBook Subscription Services
 - 4 Bit Counter Verilog Code Davefc Budget-Friendly Options
6. Navigating 4 Bit Counter Verilog Code Davefc eBook Formats
 - ePub, PDF, MOBI, and More
 - 4 Bit Counter Verilog Code Davefc Compatibility with Devices
 - 4 Bit Counter Verilog Code Davefc Enhanced eBook Features
7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of 4 Bit Counter Verilog Code Davefc
 - Highlighting and Note-Taking 4 Bit Counter Verilog Code Davefc
 - Interactive Elements 4 Bit Counter Verilog Code Davefc
8. Staying Engaged with 4 Bit Counter Verilog Code Davefc
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers 4 Bit Counter Verilog Code Davefc
9. Balancing eBooks and Physical Books 4 Bit Counter Verilog Code Davefc
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection 4 Bit Counter Verilog Code Davefc
10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
11. Cultivating a Reading Routine 4 Bit Counter Verilog Code Davefc
 - Setting Reading Goals 4 Bit Counter Verilog Code Davefc
 - Carving Out Dedicated Reading Time

12. Sourcing Reliable Information of 4 Bit Counter Verilog Code Davefc
 - Fact-Checking eBook Content of 4 Bit Counter Verilog Code Davefc
 - Distinguishing Credible Sources
13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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