

Wavelet Packet-Based Spectrum Sensing For Cognitive Radio Networks: A Matlab-Based Comparative Analysis

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ABSTRACT

This paper provides a complete MATLAB numerical and graphical study of the WPT-based spectrum sensing for cognitive radio networks. The Daubechies-4 was selected for sub-band decomposition and the signal was decomposed at 4 levels resulting in 16 sub-bands. The analysis of sub-band energy showed that the highest energy present is found in Sub-band 0 (120), and the other values were much lower (<20), therefore Sub-band 0 is most likely referring to the Primary User (PU). This result demonstrates that the detection performance of WPT ($P_d = 0.85$, $P_f = 0.15$) is better than that of energy detection ($P_d = 0.75$, $P_f = 0.20$), while it approaches the performance of cyclo-stationary detection ($P_d = 0.92$, $P_f = 0.10$) with a cutoff 60. The time-frequency heatmap and binary decision output indicate WPT becomes a reliable method to localizing both time and frequency spectrum of PU. These findings indicate that both dynamic spectrum allocation and real-time sensing frameworks can greatly improve quality-of-service while minimizing disruption to primary users. It is also worth mentioning that WPT managed to obtain a reasonable execution time of 0.45 seconds, which proves to be a good compromise between detection accuracy and computational efficiency. In general, the results confirm the suitability of WPT for dynamic spectrum access in cognitive radio settings.

Keywords: WPT, Cognitive Radio Networks, Spectrum Sensing, MATLAB

Date of Submission: 13-05-2025

Date of acceptance: 27-05-2025

I. INTRODUCTION

Advancements in communication technology have increasingly demanded efficient and reliable spectrum sensing techniques to optimize the use of available frequency bands. Cognitive Radio Networks (CRNs) have emerged as a promising solution by dynamically accessing underutilized spectrum, thereby enhancing communication efficiency [1]. A critical challenge within CRNs lies in accurately detecting spectrum availability under diverse and often uncertain noise conditions commonly encountered in real-world environments. Wavelet packet-based spectrum analysis offers a refined approach to signal decomposition and feature extraction, enabling improved detection performance compared to traditional methods. By leveraging adaptive algorithms and advanced signal processing techniques, such as those integrating differential entropy and machine learning classifiers, researchers have significantly enhanced spectrum sensing accuracy and robustness [2]. The integration of CRNs with emerging 5G technologies underscores the urgency of robust spectrum frameworks capable of supporting diverse applications and high data rates. Such advancements highlight the importance of adaptive spectrum management to sustain efficient, reliable wireless communication networks [3]. The advancement of cognitive radio networks necessitates robust tools for evaluating and comparing spectrum sensing techniques to optimize performance. Effective spectrum management in CRNs is crucial to address challenges such as spectrum scarcity, interference mitigation, and quality-of-service (QoS) maintenance. Advanced frameworks incorporating real-time sensing and dynamic spectrum allocation have proven essential for optimizing spectrum use while protecting licensed incumbents [4]. MATLAB serves as an ideal platform for this purpose due to its extensive signal processing libraries and simulation capabilities, allowing researchers to implement complex algorithms such as wavelet packet-based spectrum analysis with precision and flexibility [5]. This study explores how well

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conventional method for designing surface finish as per is 696 surface texture specified by indicating the following a roughness value i e ra value in mm b machining allowance in mm c sampling length or instrument cut off length in mm d machining production method and e direction of lay in the symbol form as x m c r

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for jis symbols specify roughness ra roughness rz rmax for gost symbols you can also select use for notation displays the surface finish symbol 0 5 times larger than the default size add default symbol displays the default surface finish symbol in parentheses format use document font

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bs en iso 1302 2002 geometrical product specifications gps indication of surface texture in technical product documentation for notes on surface roughness use link surface roughness notes the symbol indicates the surface finish requirements and shows a machining allowance requirement of 3mm on all surfaces

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let s take a look how the jis defines each type of plating such as chrome plating and zinc plating the jis defines the types grades and symbols for electro galvanizing as shown in the table below

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surface symbol symbol indicating a surface where removal processes are prohibited symbol indicating a surface that requires a removal process examples of indicating the ra upper limit a b c example of indicating grain direction examples of indicating ra upper limit and lower limit a b examples of indicating the machining method

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surface finish symbols you can specify the surface texture of a part face by using a surface finish symbol you can select the face in a part assembly or drawing document surface finish symbols are formed by combining the symbol and lay direction direction of lay

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to open the surface finish propertymanager do one of the following insert a new surface finish symbol click surface finish on the annotation toolbar or click insert annotations surface finish symbol select an existing surface finish symbol

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web as an alternative you can also write your simulation stimulus using generic vhdl code called a testbench the testbench codes gets compiled along with the design so that the stimulus is also in the compiled simulation model ieee came along and created additional libraries that are supported by almost all vhdl compilers specific silicon

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web for sample syntax and a list of vhdl statements supported by the vhdl synthesizer see appendix a quick reference for a list of exceptions and constraints on the vhdl synthesizer s support of vhdl see appendix b limitations this chapter shows you the structure of a vhdl design and then

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web basic logic gates esd chapter 2 figure 2 3 every vhdl design description consists of at least one entity architecture pair or one entity with multiple architectures the entity section of the hdl design is used to declare the i o ports of the circuit while the description code resides within architecture portion

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