FPGA Implementations of Neural Networks

Edited by

Amos R. Omondi and Jagath C. Rajapakse

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Fpga Implementations Of Neural Networks

Jicheng Xie

Fpga Implementations Of Neural Networks:

  FPGA Implementations of Neural Networks Amos R. Omondi,Jagath C. Rajapakse,2006-10-04 During the 1980s and early 1990s there was signi cant work in the design and implementation of hardware neurocomputers Nevertheless most of these efforts may be judged to have been unsuccessful at no time have have ha ware neurocomputers been in wide use This lack of success may be largely attributed to the fact that earlier work was almost entirely aimed at developing custom neurocomputers based on ASIC technology but for such niche eas this technology was never suf ciently developed or competitive enough to justify large scale adoption On the other hand gate arrays of the period m tioned were never large enough nor fast enough for serious arti cial neur network ANN applications But technology has now improved the capacity and performance of current FPGAs are such that they present a much more realistic alternative Consequently neurocomputers based on FPGAs are now a much more practical proposition than they have been in the past This book summarizes some work towards this goal and consists of 12 papers that were selected after review from a number of submissions The book is nominally divided into three parts Chapters 1 through 4 deal with foundational issues Chapters 5 through 11 deal with a variety of implementations and Chapter 12 looks at the lessons learned from a large scale project and also reconsiders design issues in light of current and future technology   FPGA Implementations of Neural Networks Amos R. Omondi,Jagath C. Rajapakse,2008-11-01 During the 1980s and early 1990s there was signi cant work in the design and implementation of hardware neurocomputers Nevertheless most of these efforts may be judged to have been unsuccessful at no time have have ha ware neurocomputers been in wide use This lack of success may be largely attributed to the fact that earlier work was almost entirely aimed at developing custom neurocomputers based on ASIC technology but for such niche eas this technology was never suf ciently developed or competitive enough to justify large scale adoption On the other hand gate arrays of the period m tioned were never large enough nor fast enough for serious arti cial neur network ANN applications But technology has now improved the capacity and performance of current FPGAs are such that they present a much more realistic alternative Consequently neurocomputers based on FPGAs are now a much more practical proposition than they have been in the past This book summarizes some work towards this goal and consists of 12 papers that were selected after review from a number of submissions The book is nominally divided into three parts Chapters 1 through 4 deal with foundational issues Chapters 5 through 11 deal with a variety of implementations and Chapter 12 looks at the lessons learned from a large scale project and also reconsiders design issues in light of current and future technology   **Field Programmable Logic and Application** Jürgen Becker,Marco Platzner,Serge Vernalde,2004-08-11 This book contains the papers presented at the 14th International Conference on Field Programmable Logic and Applications FPL held during August 30th September 1st 2004 The conference was hosted by the Interuniversity Micro Electronics Center IMEC in Leuven Belgium The FPL series of conferences was founded in 1991 at Oxford University UK and has been held annually since in

Oxford 3 times Vienna Prague Darmstadt London Tallinn Glasgow Villach Belfast Montpellier and Lisbon It is the largest and oldest conference in reconfigurable computing and brings together academic researchers industry experts users and newcomers in an informal welcoming atmosphere that encourages productive exchange of ideas and knowledge between the delegates The fast and exciting advances in field programmable logic are increasing steadily with more and more application potential and need New ground has been broken in architectures design techniques partial run time reconfiguration and applications of field programmable devices in several different areas Many of these recent innovations are reported in this volume The size of the FPL conferences has grown significantly over the years FPL in 2003 saw 216 papers submitted The interest and support for FPL in the programmable logic community continued this year with 285 scientific papers submitted demonstrating a 32% increase when compared to the year before The technical program was assembled from 78 selected regular papers 45 additional short papers and 29 posters resulting in this volume of proceedings The program also included three invited plenary keynote presentations from Xilinx Gilder Technology Report and Altera and three embedded tutorials from Xilinx the Universit at Karlsruhe TH and the University of Oslo   **FPGA Implementation of Reduced Precision Convolutional Neural Networks** Muhammad Mohid Nabil,2018 With the improvement in processing systems machine learning applications are finding widespread use in almost all sectors of technology Image recognition is one application of machine learning which has become widely popular with various architectures and systems aimed at improving recognition performance With classification accuracy now approaching saturation point many researchers are now focusing on resource and energy efficiency With the increased demand for learning applications in embedded devices it is of paramount importance to optimize power and energy consumption to increase utility in these low power embedded systems In recent months reduced precision neural networks have caught the attention of some researchers Reduced data width deep nets offer the potential of saving valuable resources on hardware platforms In turn these hardware platforms such as Field Programmable Gate Arrays FPGAs offer the potential of a low power system with massive parallelism increasing throughput and performance In this research we explore the implementations of a deep learning architecture on FPGA in the presence of resource and energy constraints We study reduced precision neural networks and implement one such architecture as a proof of concept We focus on binarized convolutional neural network and its implementation on FPGAs Binarized convolutional nets have displayed a classification accuracy of up to 88% with some smaller image sets such as CIFAR 10 This number is on the rise with some of the new architectures We study the tradeoff between architecture depth and its impact on accuracy to get a better understanding of the convolutional layers and their impact on the overall performance This is done from a hardware perspective giving us better insight enabling better resource allocation on FPGA fabric Zynq ZCU 102 has been used for accelerator implementation High level synthesis tool Vivado HLS from Xilinx is used for CNN definition on FPGA fabric   *Evolutionary Computing and Mobile Sustainable Networks* V. Suma,Noureddine Bouhmala,Haoxiang

Wang,2020-07-31 This book features selected research papers presented at the International Conference on Evolutionary Computing and Mobile Sustainable Networks ICECMSN 2020 held at the Sir M Visvesvaraya Institute of Technology on 20 21 February 2020 Discussing advances in evolutionary computing technologies including swarm intelligence algorithms and other evolutionary algorithm paradigms which are emerging as widely accepted descriptors for mobile sustainable networks virtualization optimization and automation this book is a valuable resource for researchers in the field of evolutionary computing and mobile sustainable networks **FPGA Implementation of PSO Algorithm and Neural Networks** Parviz Michael Palangpour,2010 This thesis describes the Field Programmable Gate Array FPGA implementations of two powerful techniques of Computational Intelligence CI the Particle Swarm Optimization algorithm PSO and the Neural Network NN Particle Swarm Optimization PSO is a popular population based optimization algorithm While PSO has been shown to perform well in a large variety of problems PSO is typically implemented in software Population based optimization algorithms such as PSO are well suited for execution in parallel stages This allows PSO to be implemented directly in hardware and achieve much faster execution times than possible in software In this thesis a pipelined architecture for hardware PSO implementation is presented Benchmark functions solved by software and FPGA hardware PSO implementations are compared NNs are inherently parallel with each layer of neurons processing incoming data independently of each other While general purpose processors have reached impressive processing speeds they still cannot fully exploit this inherent parallelism due to their sequential architecture In order to achieve the high neural network throughput needed for real time applications a custom hardware design is needed In this thesis a digital implementation of an NN is developed for FPGA implementation The hardware PSO implementation is designed using only VHDL while the NN hardware implementation is designed using Xilinx System Generator Both designs are synthesized using Xilinx ISE and implemented on the Xilinx Virtex II Pro FPGA Development Kit Abstract leaf iii **Enterprise Digital Transformation** Peter Augustine,Pethuru Raj,Sathyan Munirathinam,2022-02-17 Digital transformation DT has become a buzzword Every industry segment across the globe is consciously jumping toward digital innovation and disruption to get ahead of their competitors In other words every aspect of running a business is being digitally empowered to reap all the benefits of the digital paradigm All kinds of digitally enabled businesses across the globe are intrinsically capable of achieving bigger and better things for their constituents Their consumers clients and customers will realize immense benefits with real digital transformation initiatives and implementations The much awaited business transformation can be easily and elegantly accomplished with a workable and winnable digital transformation strategy plan and execution There are several enablers and accelerators for realizing the much discussed digital transformation There are a lot of digitization and digitalization technologies available to streamline and speed up the process of the required transformation Industrial Internet of Things IIoT technologies in close association with decisive advancements in the artificial intelligence AI space can bring forth the

desired transitions The other prominent and dominant technologies toward forming digital organizations include cloud IT edge fog computing real time data analytics platforms blockchain technology digital twin paradigm virtual and augmented reality VR AR techniques enterprise mobility and 5G communication These technological innovations are intrinsically competent and versatile enough to fulfill the varying requirements for establishing and sustaining digital enterprises Enterprise Digital Transformation Technology Tools and Use Cases features chapters on the evolving aspects of digital transformation and intelligence It covers the unique competencies of digitally transformed enterprises IIoT use cases and applications It explains promising technological solutions widely associated with digital innovation and disruption The book focuses on setting up and sustaining smart factories that are fulfilling the Industry 4 0 vision that is realized through the IIoT and allied technologies *Embedded Computer Systems: Architectures, Modeling, and Simulation* Cristina Silvano,Christian Pilato,Marc Reichenbach,2023-11-06 This book constitutes the proceedings of the 22st International Conference on Embedded Computer Systems Architectures Modeling and Simulation SAMOS 2021 which took place in July 2022 in Samos Greece The 11 full papers and 7 short papers presented in this volume were carefully reviewed and selected from 45 submissions The conference covers a wide range of embedded systems design aspects including machine learning accelerators and power management and programmable dataflow systems **Artificial Neural Networks** ,2002

Progress in Pattern Recognition, Image Analysis, Computer Vision, and Applications Eduardo Bayro-Corrochano,Edwin Hancock,2014-10-23 This book constitutes the refereed proceedings of the 19th Iberoamerican Congress on Pattern Recognition CIARP 2014 held in Puerto Vallarta Jalisco Mexico in November 2014 The 115 papers presented were carefully reviewed and selected from 160 submissions The papers are organized in topical sections on image coding processing and analysis segmentation analysis of shape and texture analysis of signal speech and language document processing and recognition feature extraction clustering and classification pattern recognition and machine learning neural networks for pattern recognition computer vision and robot vision video segmentation and tracking

Field-programmable Logic and Applications ,2000 **Understanding and Bridging the Gap between Neuromorphic Computing and Machine Learning, volume II** Huajin Tang,Lei Deng ,Kaushik Roy,2024-08-26 Towards the long standing dream of artificial intelligence two solution paths have been paved i neuroscience driven neuromorphic computing ii computer science driven machine learning The former targets at harnessing neuroscience to obtain insights for brain like processing by studying the detailed implementation of neural dynamics circuits coding and learning Although our understanding of how the brain works is still very limited this bio plausible way offers an appealing promise for future general intelligence In contrast the latter aims at solving practical tasks typically formulated as a cost function with high accuracy by eschewing most neuroscience details in favor of brute force optimization and feeding a large volume of data With the help of big data e g ImageNet high performance processors e g GPU TPU effective training algorithms e g artificial

neural networks with gradient descent training and easy to use design tools e g Pytorch Tensorflow machine learning has achieved superior performance in a broad spectrum of scenarios Although acclaimed for the biological plausibility and the low power advantage benefit from the spike signals and event driven processing there are ongoing debates and skepticisms about neuromorphic computing since it usually performs worse than machine learning in practical tasks especially in terms of the accuracy   Advances in Neural Networks--ISNN ... ,2005   Parallel Architectures for Artificial Neural Networks N. Sundararajan,P. Saratchandran,1998-12-14 An excellent reference for neural networks research and application this book covers the parallel implementation aspects of all major artificial neural network models in a single text Parallel Architectures for Artificial Neural Networks details implementations on various processor architectures built on different hardware platforms ranging from large general purpose parallel computers to custom built MIMD machine Working experts describe their implementation research including results that are then divided into three sections The theoretical analysis of parallel implementation schemes on MIMD message passing machines The details of parallel implementation of BP neural networks on general purpose large parallel computers Four specific purpose parallel neural computer configuration Aimed at graduate students and researchers working in artificial neural networks and parallel computing this work can be used by graduate level educators to illustrate parallel computing methods for ANN simulation Practitioners will also find the text an ideal reference tool for lucid mathematical analyses   **Fpga Implementation of Hopfield Neural Network** Avvaru Srinivasulu,2012-03 This work was to establish whether it was possible to achieve a reasonable speedup by implementing FPGA based Hopfield neural networks for some simple constraint satisfaction problems The results are significant our initial implementation using standard Xilinx FPGAs yielded 2 3 orders of magnitude speedup over the Sun Blade 2000 workstation comes with 1 2 GHz version of the 64 bit UltraSPARC III Cu processor The main problem with the work to date is that the problems are both unrealistically small and simplistic That is the constraints on the N Queen problem are simpler than those found in many real world scheduling applications Thus it is not clear whether we will be able to optimize the neuron structure for more complex problems since the weights matrix may not contain as many zero elements Thus a new method for speed improvement of Hopfield neural networks for solving constraint satisfaction problems using Field Programmable Gate Arrays FPGAs was proposed and implemented   ANZIIS ... ,1996   **ICICCT 2019 – System Reliability, Quality Control, Safety, Maintenance and Management** Vinit Kumar Gunjan,Vicente Garcia Diaz,Manuel Cardona,Vijender Kumar Solanki,K. V. N. Sunitha,2019-06-27 This book discusses reliability applications for power systems renewable energy and smart grids and highlights trends in reliable communication fault tolerant systems VLSI system design and embedded systems Further it includes chapters on software reliability and other computer engineering and software management related disciplines and also examines areas such as big data analytics and ubiquitous computing Outlining novel innovative concepts in applied areas of reliability in electrical electronics and computer engineering disciplines it is a valuable resource

for researchers and practitioners of reliability theory in circuit based engineering domains **Proceedings of the Fourth International Conference on Microelectronics for Neural Networks and Fuzzy Systems** ,1994 **ICANN99** ,1999 **International Symposium on Neuro-Fuzzy Systems** ,1996 This is a first conference describing advances in designing and using integrated circuits in control system The application of neural networks on VLSI is explored The Use of fuzzy logic in integrated circuit product controllers is explored

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