



# Data Retention in MLC NAND Flash Memory: Characterization, Optimization, and Recovery

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# Data Retention In Mlc Nand Flash Memory Characterization

**Ashot Martirosian-Melik**



## **Data Retention In Mlc Nand Flash Memory Characterization:**

*Constructive Side-Channel Analysis and Secure Design* Ilia Polian, Marc Stöttinger, 2019-03-15 This book constitutes revised selected papers from the 10th International Workshop on Constructive Side Channel Analysis and Secure Design COSADE 2019 held in Darmstadt Germany in April 2019 The 14 papers presented together with one keynote and one invited talk in this volume were carefully reviewed and selected from 34 submissions They were organized in topical sections named Side Channel Attacks Fault Injection Attacks White Box Attacks Side Channel Analysis Methodologies Security Aspects of Post Quantum Schemes and Countermeasures Against Implementation Attacks

**Inside Solid State Drives (SSDs)** Rino Micheloni, Alessia Marelli, Kam Eshghi, 2018-07-11 The revised second edition of this respected text provides a state of the art overview of the main topics relating to solid state drives SSDs covering NAND flash memories memory controllers including booth hardware and software I O interfaces PCIe SAS SATA reliability error correction codes BCH and LDPC encryption flash signal processing and hybrid storage Updated throughout to include all recent work in the field significant changes for the new edition include A new chapter on flash memory errors and data recovery procedures in SSDs for reliability and lifetime improvement Updated coverage of SSD Architecture and PCI Express Interfaces moving from PCIe Gen3 to PCIe Gen4 and including a section on NVMe over fabric NVMe An additional section on 3D flash memories An update on standard reliability procedures for SSDs Expanded coverage of BCH for SSDs with a specific section on detection A new section on non binary Low Density Parity Check LDPC codes the most recent advancement in the field A description of randomization in the protection of SSD data against attacks particularly relevant to 3D architectures The SSD market is booming with many industries placing a huge effort in this space spending billions of dollars in R D and product development Moreover flash manufacturers are now moving to 3D architectures thus enabling an even higher level of storage capacity This book takes the reader through the fundamentals and brings them up to speed with the most recent developments in the field and is suitable for advanced students researchers and engineers alike

Emerging Computing: From Devices to Systems Mohamed M. Sabry Aly, Anupam Chattopadhyay, 2022-07-11 The book covers a range of topics dealing with emerging computing technologies which are being developed in response to challenges faced due to scaling CMOS technologies It provides a sneak peek into the capabilities unleashed by these technologies across the complete system stack with contributions by experts discussing device technology circuit architecture and design automation flows Presenting a gradual progression of the individual sub domains and the open research and adoption challenges this book will be of interest to industry and academic researchers technocrats and policymakers Chapters Innovative Memory Architectures Using Functionality Enhanced Devices and Intelligent Edge Biomedical Sensors in the Internet of Things IoT Era are available open access under a Creative Commons Attribution 4.0 International License via [link.springer.com](http://link.springer.com)

**Semiconductor Memories and Systems** Andrea Redaelli, Fabio Pellizzer, 2022-06-07 Semiconductor Memories and Systems provides a comprehensive

overview of the current state of semiconductor memory at the technology and system levels After an introduction on market trends and memory applications the book focuses on mainstream technologies illustrating their current status challenges and opportunities with special attention paid to scalability paths Technologies discussed include static random access memory SRAM dynamic random access memory DRAM non volatile memory NVM and NAND flash memory Embedded memory and requirements and system level needs for storage class memory are also addressed Each chapter covers physical operating mechanisms fabrication technologies and the main challenges to scalability Finally the work reviews the emerging trends for storage class memory mainly focusing on the advantages and opportunities of phase change based memory technologies Features contributions from experts from leading companies in semiconductor memory Discusses physical operating mechanisms fabrication technologies and paths to scalability for current and emerging semiconductor memories Reviews primary memory technologies including SRAM DRAM NVM and NAND flash memory Includes emerging storage class memory technologies such as phase change memory

**CMOS Plasma and Process Damage** Kirk Prall,2025-05-16 This book discusses the complex technology of building CMOS computer chips and covers some of the unusual problems that can occur during chip manufacturing Readers will learn how plasma and process damage results from the high energy processes that are used in chip manufacturing causing harm to the chips functional failure and reliability problems

**Advances in Computers** ,2019-05-22 Advances in Computers Volume 114 the latest volume in this innovative series published since 1960 presents detailed coverage of new advancements in computer hardware software theory design and applications Chapters in this updated release include A Comprehensive Survey of Issues in Solid State Drives Revisiting VM performance and optimization challenges for big data Towards Realizing Self Protecting Healthcare Information Systems Design and Security Challenges and SSIM and ML based QoE enhancement approach in SDN context Provides in depth surveys and tutorials on new computer technology Covers well known authors and researchers in the field Presents extensive bibliographies with most chapters Includes volumes that are devoted to single themes or subfields of computer science

**Nanometer CMOS ICs** Harry Veendrick,2024-10-21 This textbook provides a comprehensive fully updated introduction to the essentials of nanometer CMOS integrated circuits It includes aspects of scaling to even beyond 3nm CMOS technologies and designs It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design fabrication and application Coverage includes all associated disciplines of nanometer CMOS ICs including physics lithography technology design memories VLSI power consumption variability reliability and signal integrity testing yield failure analysis packaging scaling trends and road blocks The text is based upon in house Philips NXP Semiconductors Applied Materials ASML IMEC ST Ericsson Infineon TSMC etc courseware which to date has been completed by more than 7000 engineers working in a large variety of the above mentioned disciplines

Nanometer CMOS ICs Harry J.M. Veendrick,2017-04-28 This textbook provides a comprehensive fully updated introduction to the essentials of nanometer

CMOS integrated circuits It includes aspects of scaling to even beyond 12nm CMOS technologies and designs It clearly describes the fundamental CMOS operating principles and presents substantial insight into the various aspects of design implementation and application Coverage includes all associated disciplines of nanometer CMOS ICs including physics lithography technology design memories VLSI power consumption variability reliability and signal integrity testing yield failure analysis packaging scaling trends and road blocks The text is based upon in house Philips NXP Semiconductors Applied Materials ASML IMEC ST Ericsson TSMC etc courseware which to date has been completed by more than 4500 engineers working in a large variety of related disciplines architecture design test fabrication process packaging failure analysis and software

**EDN, Electrical Design News** ,2002 *NAND Flash Memory* Yu Cai,2013 **NAND Flash Memory Technologies** Seiichi Aritome,2015-11-30 Offers a comprehensive overview of NAND flash memories with insights into NAND history technology challenges evolutions and perspectives Describes new program disturb issues data retention power consumption and possible solutions for the challenges of 3D NAND flash memory Written by an authority in NAND flash memory technology with over 25 years experience

**Case-Specific Lifetime Management Strategies for Long-Lasting Flash Devices** Wonil Choi,2021 NAND flash memory based devices have limited lifetime which should be carefully and effectively managed for a longer use This is because flash lifetime is non renewable consumable a flash memory can process only a finite fixed number of write erase operations beyond which it becomes unreliable One traditional straightforward way of improving flash lifetime is to employ data deduplication and or compression techniques which can reduce the size of original data to be written into the device and thus cut the use of limited number of write erase operations compared to when such techniques are absent in processing the same amount of data While these flash agnostic techniques are effective to some extent one can potentially explore further opportunities to improve flash lifetime if unique characteristics of target flash devices and or target workload execution scenarios are taken into account Considering various execution scenarios and workload types a flash device can encounter this dissertation presents case specific lifetime enhancement strategies for flash memory based storage systems Specifically this dissertation focuses on three different cases frequently faced in practice i when target flash device employs Single Level Cell SLC technology and executes a single workload ii when target device employs Multi Level Cell MLC technology and executes a single workload and iii when target device executes multiple co running workloads regardless of its employed flash technology For case i based on our observation that data longevity i e time between two consecutive writes updates on the same data is generally short in many flash destined workloads we propose a strategy that attempts to relax long retention times the time to secure the data error free of SLC memory cells The relaxation of retention times in an SLC memory cell can enable the service of multiple write operations per a single erase operation thereby improving device lifetime Regarding case ii motivated by the observation that multiple data can be accommodated in each MLC memory cell and this is realized by several voltage states within it we

propose a strategy that attempts to conserve the multiple voltage states i.e. consumes the available states densely or compactly Using the multiple voltage states originally for securing more storage capacity for the service of multiple write operations per a single erase operation can enhance device lifetime in scenarios where there is no need of such a large storage capacity As for case iii motivated by our observation that the state of the art over provisioned OP flash capacity partitioning strategies are not optimal from a device lifetime angle while they certainly help to provide a guaranteed service level to each of co running workload we propose a strategy using which one can explore the OP partitioning space and determine a lifetime optimal OP partitioning that minimizes the collective number of write operations coming from garbage collection GC thus maximizing device lifetime Our extensive experimental evaluations based on simulation I/O traces from real workloads for cases i and ii and emulation real applications for case iii demonstrate that our proposed techniques i ii and iii can improve the device lifetime by 6.8x 27.9% and 43% on average respectively against a conventional SLC flash a conventional MLC flash and a state of the art lifetime agnostic OP partitioning strategy Also all our proposed approaches lead to improved performance e.g. response time and throughput or provide at least the same level of performance when compared to a baseline that does not consider device lifetime explicitly

Characterization of TLC Flash Memory Zachary Taylor Blair, 2017 Flash memory manufacturers are increasing storage density by leveraging multi bit per cell NAND flash technology in the latest process nodes Error rates and endurance can be significantly altered in each generation and the manufacturers provide conservative guidelines for these metrics Deeper understanding of the physical characteristics of flash devices can be used to develop a usage model which improves lifetime and reliability We developed a System on Chip SoC platform for flash memory testing including a hardware memory controller and software for pattern generation and data processing We have used the platform to characterize properties of a Triple Level Cell TLC flash memory device from a single vendor and found behaviors have significantly changed from previous generations Among these novel findings manufacturers have built compensation mechanisms for some worst case behaviors such as inter cell interference ICI but other effects become inherently more significant in the latest technologies With information about how certain behaviors affect reliability in both the short term and toward the end of the product lifetime this work provides speculation on the goals for coding schemes which target error mitigation

Inside NAND Flash Memories Rino Micheloni, Luca Crippa, Alessia Marelli, 2010-07-27 Digital photography MP3 digital video etc make extensive use of NAND based Flash cards as storage media To realize how much NAND Flash memories pervade every aspect of our life just imagine how our recent habits would change if the NAND memories suddenly disappeared To take a picture it would be necessary to find a film as well as a traditional camera disks or even magnetic tapes would be used to record a video or to listen a song and a cellular phone would return to be a simple mean of communication rather than a multimedia console The development of NAND Flash memories will not be set down on the mere evolution of personal entertainment systems since a new killer application can

trigger a further success the replacement of Hard Disk Drives HDDs with Solid State Drives SSDs SSD is made up by a microcontroller and several NANDs As NAND is the technology driver for IC circuits Flash designers and technologists have to deal with a lot of challenges Therefore SSD system developers must understand Flash technology in order to exploit its benefits and countermeasure its weaknesses Inside NAND Flash Memories is a comprehensive guide of the NAND world from circuits design analog and digital to Flash reliability including radiation effects from testing issues to high performance DDR interface from error correction codes to NAND applications like Flash cards and SSDs Flash Memory Characterization Ashot Martirosian-Melik,2002 Endurance Characterization and Improvement of Floating Gate Semiconductor Memory Devices Faraz I. Khan,2009 Low power consumption virtually zero latency extremely fast boot up for OS and applications fast data access portability and high shock resistance are some of many reasons that make Flash memory devices an ideal choice for a vast variety of consumer electronics Flash memory is a specific type of non volatile EEPROM A typical Flash memory cell looks similar to a MOSFET except that it has a dual gate structure Flash memory cells use the principle of threshold voltage modulation to alter the channel current  $I_{ds}$  when a reference read voltage  $V_{read}$  is applied to the control gate Different levels of  $I_{ds}$  are in turn interpreted as unique logic states Fowler Nordheim tunneling is used to achieve threshold voltage modulation in NAND Flash memory cells Despite its high performance potential NAND Flash memory suffers from the drawback of limited program erase endurance High field current stress caused by Fowler Nordheim tunneling during program erase cycling leads to tunnel oxide degradation which eventually limits the endurance characteristics of NAND Flash memory cells One of the most significant tunnel oxide degradation mechanisms is charge trapping This work is devoted to the study of charge trapping and its effects on the endurance characteristics and reliability of NAND Flash memory devices Cell threshold voltage shift and memory window narrowing a direct consequence of tunnel oxide degradation caused by charge trapping are typical failure modes in NAND Flash memory cells In this work endurance characterization of NAND Flash memory devices and a detailed analysis has been conducted reconfirming the issue of limited program erase endurance Subsequently a novel NAND Flash memory cell design has been proposed which eliminates tunnel oxide degradation caused by Fowler Nordheim tunneling Device simulations using the Sentaurus TCAD tool suite by Synopsys Inc and corresponding analysis show that as compared to conventional cells the proposed cell design offers a 10 times reduction in intrinsic threshold voltage shift That according to the measured endurance characteristics of cells fabricated in this work translates to an improvement of over 200 times in program erase endurance In a nutshell the proposed cell design offers superior reliability and endurance as compared to conventional NAND Flash memory cells

**Resistive Random Access Memory** Liang Zhao,2015 Recently the rapid development of big data and internet of things has fueled a surge of demand for semiconductor memories As the scaling of NAND flash is hitting its physical limits several emerging non volatile memory technologies are being studied intensively to enable higher memory density and better

performance Among them resistive random access memory RRAM has attracted tremendous interests due to its ability to overcome the inherent limitations of flash memory while also delivering cost effectiveness robust performance and small footprint Despite its promising features several challenges remain to be addressed for the future development and commercialization of RRAM technology First of all the physical mechanisms behind resistance change phenomena have not been fully understood making it difficult to optimize the device performance Secondly the reliability of RRAM should be improved in several aspects such as the variability of switching parameters the retention endurance failures caused by the random nature of filament formation as well as the requirement for a high voltage forming process Moreover it is also highly desired to stack RRAM devices in a 3D architecture and or develop multi level storage capability to reduce the cost per bit and compete with NAND flash This thesis presents an in depth analysis of some state of the art techniques to tackle these challenges from three aspects the materials the device structure as well as the characterization methods From the material s perspective doping technology of RRAM is investigated as an approach to improve RRAM performance Ab initio modeling and simulations are applied to study the effects of dopant types dopant concentrations oxide phases and oxide stoichiometry on the electronic and thermodynamic properties of oxygen vacancies in HfO<sub>2</sub> The physical insights derived from the calculations provide guidelines to achieve desirable RRAM characteristics through doping In the aspect of electrical characterization the pulse train characterization techniques are developed for the multi level control and in depth physical understanding of conductive filament evolution By adopting pulse train operation for an RRAM device with 3 bit potential the relative standard deviations of resistance levels are improved up to 80% compared to the single pulse scheme The observed exponential relation between the saturated resistance and the pulse amplitude provides supporting evidence for the gap formation model during the RESET process of RRAM From the device structure point of view the feasibility of ultra thin HfO<sub>2</sub> RRAM is investigated which helps to achieve the forming free property and low power operation The theoretical scaling limit of HfO<sub>x</sub> thickness is first estimated using density functional theory within the non equilibrium Green s function formalism The feasibility of 2 nm HfO<sub>x</sub> RRAM is predicted for large area devices and verified by fabricating both planar and 3D vertical RRAM devices The 3D ultra thin devices demonstrate promising characteristics including ON OFF ratio 100 switching speed 20 ns endurance 10<sup>8</sup> cycles and data retention 10 years at room temperature In contributing to these areas this thesis aims at advancing both the fundamental understanding and practical implementation of RRAM technology towards the vision of high density mass storage applications

**3D Flash Memories** Rino Micheloni, 2016-05-26 This book walks the reader through the next step in the evolution of NAND flash memory technology namely the development of 3D flash memories in which multiple layers of memory cells are grown within the same piece of silicon It describes their working principles device architectures fabrication techniques and practical implementations and highlights why 3D flash is a brand new technology After reviewing market trends for both NAND and solid state drives SSDs the book digs into the details of the flash memory

cell itself covering both floating gate and emerging charge trap technologies There is a plethora of different materials and vertical integration schemes out there New memory cells new materials new architectures 3D Stacked BiCS and P BiCS 3D FG 3D VG 3D advanced architectures basically each NAND manufacturer has its own solution Chapter 3 to chapter 7 offer a broad overview of how 3D can materialize The 3D wave is impacting emerging memories as well and chapter 8 covers 3D RRAM resistive RAM crosspoint arrays Visualizing 3D structures can be a challenge for the human brain this is way all these chapters contain a lot of bird s eye views and cross sections along the 3 axes The second part of the book is devoted to other important aspects such as advanced packaging technology i e TSV in chapter 9 and error correction codes which have been leveraged to improve flash reliability for decades Chapter 10 describes the evolution from legacy BCH to the most recent LDPC codes while chapter 11 deals with some of the most recent advancements in the ECC field Last but not least chapter 12 looks at 3D flash memories from a system perspective Is 14nm the last step for planar cells Can 100 layers be integrated within the same piece of silicon Is 4 bit cell possible with 3D Will 3D be reliable enough for enterprise and datacenter applications These are some of the questions that this book helps answering by providing insights into 3D flash memory design process technology and applications

#### **Resistive Random Access Memory (RRAM)** Shimeng Yu,2022-06-01

RRAM technology has made significant progress in the past decade as a competitive candidate for the next generation non volatile memory NVM This lecture is a comprehensive tutorial of metal oxide based RRAM technology from device fabrication to array architecture design State of the art RRAM device performances characterization and modeling techniques are summarized and the design considerations of the RRAM integration to large scale array with peripheral circuits are discussed Chapter 2 introduces the RRAM device fabrication techniques and methods to eliminate the forming process and will show its scalability down to sub 10 nm regime Then the device performances such as programming speed variability control and multi level operation are presented and finally the reliability issues such as cycling endurance and data retention are discussed Chapter 3 discusses the RRAM physical mechanism and the materials characterization techniques to observe the conductive filaments and the electrical characterization techniques to study the electronic conduction processes It also presents the numerical device modeling techniques for simulating the evolution of the conductive filaments as well as the compact device modeling techniques for circuit level design Chapter 4 discusses the two common RRAM array architectures for large scale integration one transistor one resistor 1T1R and cross point architecture with selector The write read schemes are presented and the peripheral circuitry design considerations are discussed Finally a 3D integration approach is introduced for building ultra high density RRAM array Chapter 5 is a brief summary and will give an outlook for RRAM s potential novel applications beyond the NVM applications

*Radiation Characterization of Highly Integrated NAND-Flash Memory Devices for Spaceborne Mass Storage Applications* Kai Grürmann,2015

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