

# Digital Electronics

## CHARACTERISTICS OF LOGIC FAMILY



### PROPAGATION DELAY (t<sub>pd</sub>)

Measured in nano seconds (ns)

Time taken for signal to propagate from input to output.

Time taken for signal to propagate from input to output (t<sub>rise</sub> > t<sub>fall</sub>) due to storage time or calculation delay.



Due to the propagation delay in the gates, the output signal is not exactly identical to the input signal. When the input is applied.



$$t_{pd} = \frac{t_{rise} + t_{fall}}{2}$$

In reality, transition changes (transitions from 0 to 1 or vice versa) doesn't happen instantaneously. Sometimes it spent some time in between (0.5 or 0.5).

All logic family is the fastest among all.

### POWER DISSIPATION

Power dissipation is power dissipated by a logic gate.

Measured in milliwatts (mW)

Mathematically

$$P_{diss} = V_{cc} \times I_{c(avg)}$$

$$I_{c(avg)} = \frac{I_c(0) + I_c(1)}{2}$$

I<sub>c(0)</sub> = I<sub>c</sub> (low)

I<sub>c(1)</sub> = I<sub>c</sub> (high)

CMOS logic family has lowest power dissipation.

I<sub>c(0)</sub> should be zero, but practically low current.



$$I_{c(sat)} = \frac{V_{cc} - V_{ce(sat)}}{R_c}$$

$$I_{c(0)} = \frac{V_{cc}}{R_c}$$

### FIGURE OF MERIT

Mathematically

$$F.O.M = t_{pd} \times P_{diss}$$

$$= ns \times mW$$

$$= pJ \text{ (Picjoules)}$$

$$CMOS = 0.1 pJ \text{ to } 0.7 pJ$$

Best F.O.M is for CMOS logic family among all logic families. CMOS has F.O.M in range of 0.1 pJ to 0.7 pJ.

# Digital Electronics Lecture Notes 2011 2012

**Camilla Rothe**



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## **Table of Contents Digital Electronics Lecture Notes 2011 2012**

1. Understanding the eBook Digital Electronics Lecture Notes 2011 2012
  - The Rise of Digital Reading Digital Electronics Lecture Notes 2011 2012
  - Advantages of eBooks Over Traditional Books
2. Identifying Digital Electronics Lecture Notes 2011 2012
  - Exploring Different Genres
  - Considering Fiction vs. Non-Fiction
  - Determining Your Reading Goals
3. Choosing the Right eBook Platform
  - Popular eBook Platforms
  - Features to Look for in an Digital Electronics Lecture Notes 2011 2012
  - User-Friendly Interface
4. Exploring eBook Recommendations from Digital Electronics Lecture Notes 2011 2012
  - Personalized Recommendations
  - Digital Electronics Lecture Notes 2011 2012 User Reviews and Ratings
  - Digital Electronics Lecture Notes 2011 2012 and Bestseller Lists

5. Accessing Digital Electronics Lecture Notes 2011 2012 Free and Paid eBooks
  - Digital Electronics Lecture Notes 2011 2012 Public Domain eBooks
  - Digital Electronics Lecture Notes 2011 2012 eBook Subscription Services
  - Digital Electronics Lecture Notes 2011 2012 Budget-Friendly Options
6. Navigating Digital Electronics Lecture Notes 2011 2012 eBook Formats
  - ePub, PDF, MOBI, and More
  - Digital Electronics Lecture Notes 2011 2012 Compatibility with Devices
  - Digital Electronics Lecture Notes 2011 2012 Enhanced eBook Features
7. Enhancing Your Reading Experience
  - Adjustable Fonts and Text Sizes of Digital Electronics Lecture Notes 2011 2012
  - Highlighting and Note-Taking Digital Electronics Lecture Notes 2011 2012
  - Interactive Elements Digital Electronics Lecture Notes 2011 2012
8. Staying Engaged with Digital Electronics Lecture Notes 2011 2012
  - Joining Online Reading Communities
  - Participating in Virtual Book Clubs
  - Following Authors and Publishers Digital Electronics Lecture Notes 2011 2012
9. Balancing eBooks and Physical Books Digital Electronics Lecture Notes 2011 2012
  - Benefits of a Digital Library
  - Creating a Diverse Reading Collection Digital Electronics Lecture Notes 2011 2012
10. Overcoming Reading Challenges
  - Dealing with Digital Eye Strain
  - Minimizing Distractions
  - Managing Screen Time
11. Cultivating a Reading Routine Digital Electronics Lecture Notes 2011 2012
  - Setting Reading Goals Digital Electronics Lecture Notes 2011 2012
  - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Digital Electronics Lecture Notes 2011 2012
  - Fact-Checking eBook Content of Digital Electronics Lecture Notes 2011 2012
  - Distinguishing Credible Sources
13. Promoting Lifelong Learning

- Utilizing eBooks for Skill Development
  - Exploring Educational eBooks
14. Embracing eBook Trends
- Integration of Multimedia Elements
  - Interactive and Gamified eBooks

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