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QPSK Modulator and Demodulator Using FPGA for SDR

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ABSTRACT
A software-defined radio (SDR) allows for digital communication systems to simply accept more complicated coding and modulation technologies, which is enormously vital in meeting the ever-increasing demands of the wireless communication industry. An SDR has been constructed, using the Simulink tool, and implemented on the SPARTEN-3E Field Programmable Gate Array (FPGA) development kit. The modulation scheme used in the system is Quadrature Phase-Shift Keying (QPSK). In the first step to realize the whole modulation and demodulation schemes using MATLAB Simulink. The format of a VHDL program is built around the concept of BLOCKS which are the basic building units of a VHDL design. The results showed that the proposed method can greatly improve the developing efficiency, shorten developing period and reduce costs.
Keywords - Demodulator, FPGA, Modulator, QPSK, SDR VHDL.

I. INTRODUCTION

The objective of this paper is to design a QPSK modem using FPGA for SDR (Software Defined Radio). In this paper the modulator and demodulator is implemented on single FPGA kit. In which mainly concentrates on QPSK modulation techniques. In QPSK, two successive bits sequence are grouped together, this reduces the bit rate of a signaling rate (f_s) and reduces the bandwidth of the channel.

Quadrature Phase Shift Keying (QPSK) modulation ordinary used modem chips or ASICS, to implement, but those chips usually do not have sufficient programming skill and its functionality cannot easily be changed or improved in the product development process. So those chips are not suitable the situation where the parameters changed frequently. The communication system based on FPGA is easy to implement the pipeline architecture and simple to upgrade. This is a very practical approach to implement the QPSK modulator and demodulator [1].

The FPGA implementation of π4 QPSK modulator and demodulator is presented complete modulator and demodulator units will be modeled using VHDL and functionality will be verified using modelsim simulation tools. The code will be synthesized onto Xilinx FPGA kit. The modulator consists of various communication modules like phase calculator, I-Q mapper, frequency synthesizer, clock generator and COS-LUT. The demodulator consists of modules COS-LUT, Negative SIN-LUT, digital multiplier integrate and dump circuit and baseband differential detector. These digital modules

will be implemented as different modules and used as components in top level entities [2].

II. THE MODULATOR AND DEMODULATOR ARCHITECTURE

Principle of QPSK modulator— in quadrature phase shift keying (QPSK), two successive bits in the data sequence are grouped together this reduces the bit rate of a signaling rate (f_s) and hence reduces the bandwidth of the channel. QPSK Modulator— the modulator converts the input bit stream into an electrical waveforms suitable for transmission over the communication channel. Modulator is used to minimize the effect of channel noise and matching the frequency spread spectrum of transmitted signal.
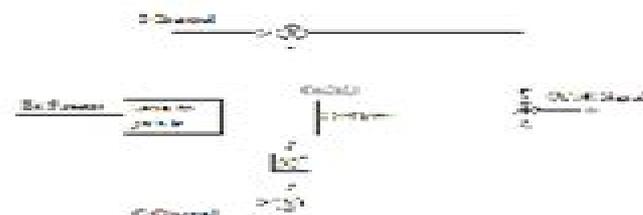

Fig (1): Block diagram of QPSK Modulator

The above fig (1) shows a block diagram of typical QPSK transmitter. The unipolar binary message stream has bit rate R_b and is first converted into a bipolar non-return-to-zero (NRZ) sequence using a unipolar to bipolar converter. The bit stream

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FM will need to be supported in such systems A challenge that comes with programming FPGAs is the increased design and implementation time over conventional software programming In this thesis three FM demodulator techniques are implemented and compared in an FPGA Two techniques are found to have similar SNR performance while having very different FPGA implementation characteristics Library based design is explored for demodulators to increase FPGA design productivity A block library is created and verified by use in tested demodulator designs Two design tools that aim to increase design productivity in FPGAs Ogre and HMFlow are also examined and used to implement FM demodulators in a PCM FM receiver design Ogre leverages the demodulator block library along with accompanying metadata to decrease design time significantly Design performance is not sacrificed when using Ogre HMFlow which relies on finer grained blocks reuses block implementation data to speed up implementation of the full design The implementation of the HMFlow demodulator design is sped up by 3x but when compared with the standard flow produces an implementation with a reduced maximum clock rate about 1 2 and with slightly more resources about 6% When comparing Ogre with HMFlow the coarser grained blocks of Ogre provide a more efficient design experience than that of HMFlow **Design and Implementation of Discrete Multitone Modulator Using FPGA** Hadi T. Ziboon,Ikhlas M. Farhan,2014-04 The aim of the book is to design simulation and implementation of the Discrete Multitone DMT modulation for ADSL based on Software Defined Radio SDR using FPGA DMT divides the available bandwidth into parallel sub channels The main units of the DMT modulator are serial to parallel converter symbol mapping IFFT parallel to serial and cyclic prefix There are two techniques to transmit data namely complex transmission and real transmission Real transmission is preferred for DSL since it needs single wire but uses twice number of IFFT *M-ary Amplitude Shift Keying-orthogonal Frequency Division Multiplexing Modulator and Demodulator Implementation Using FPGA* Haiying Deng,2001 Remodulation-based QPSK Demodulator with Decision Feedback P. Catapano,1997

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