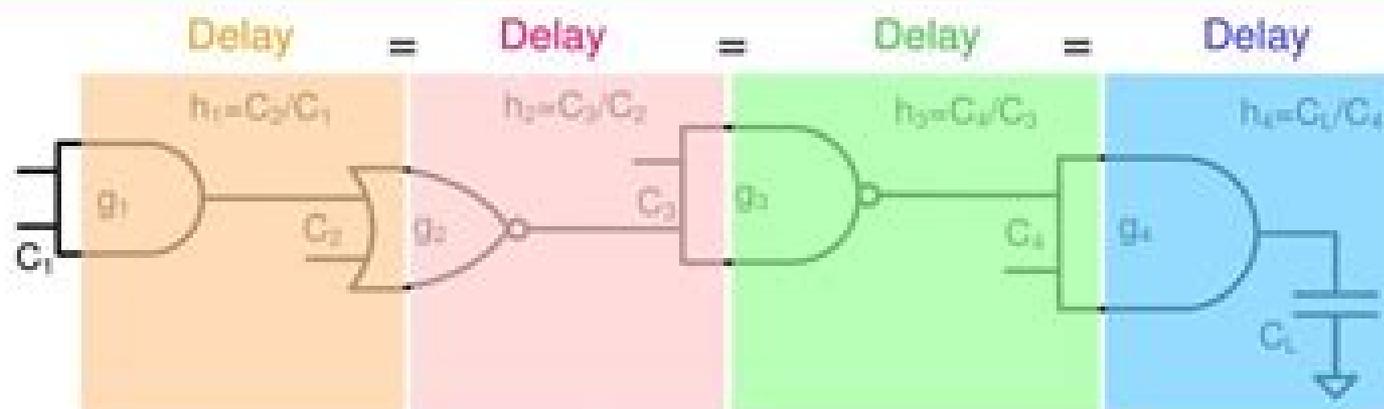


# Logical Effort (*only logic*)



*Delay model*

*Optimal sizing*

$$D_i = \tau \cdot g_i \cdot h_i + p_i$$

$$\text{Delay}_i = \text{Delay}_{i+1}$$

$\tau$  - delay of minimal inverter  $R_0 \cdot C_0$ , technology constant

$g_i$  - logical effort, gate type factor: e.g.  $g_{inv} = 1$

$h_i$  - electrical effort, load driving capability

$p_i$  - parasitic effort, due to output capacitance

$$g_i h_i = g_{i+1} h_{i+1}$$

# [Download Logical Effort Designing Fast Cmos Circuits](#)

**Christian Piguet**



## **Download Logical Effort Designing Fast Cmos Circuits:**

**Logical Effort** Ivan Sutherland, Robert F. Sproull, David Harris, 1999 Designers of high speed integrated circuits face a bewildering array of choices and too often spend frustrating days tweaking gates to meet speed targets Logical Effort Designing Fast CMOS Circuits makes high speed design easier and more methodical providing a simple and broadly applicable method for estimating the delay resulting from factors such as topology capacitance and gate sizes The brainchild of circuit and computer graphics pioneers Ivan Sutherland and Bob Sproull logical effort will change the way you approach design challenges This book begins by equipping you with a sound understanding of the method s essential procedures and concepts so you can start using it immediately Later chapters explore the theory and finer points of the method and detail its specialized applications Features Explains the method and how to apply it in two practically focused chapters Improves circuit design intuition by teaching simple ways to discern the consequences of topology and gate size decisions Offers easy ways to choose the fastest circuit from among an array of potential circuit designs Reduces the time spent on tweaking and simulations so you can rapidly settle on a good design Offers in depth coverage of specialized areas of application for logical effort skewed or unbalanced gates other circuit families including pseudo NMOS and domino wide structures such as decoders and irregularly forking circuits Presents a complete derivation of the method so you see how and why it works

**CMOS Processors and Memories** Krzysztof Iniewski, 2010-08-09 CMOS Processors and Memories addresses the state of the art in integrated circuit design in the context of emerging computing systems New design opportunities in memories and processor are discussed Emerging materials that can take system performance beyond standard CMOS like carbon nanotubes graphene ferroelectrics and tunnel junctions are explored CMOS Processors and Memories is divided into two parts processors and memories In the first part we start with high performance low power processor design followed by a chapter on multi core processing They both represent state of the art concepts in current computing industry The third chapter deals with asynchronous design that still carries lots of promise for future computing needs At the end we present a hardware design space exploration methodology for implementing and analyzing the hardware for the Bayesian inference framework This particular methodology involves analyzing the computational cost and exploring candidate hardware components proposing various custom architectures using both traditional CMOS and hybrid nanotechnology CMOL The first part concludes with hybrid CMOS Nano architectures The second memory part covers state of the art SRAM DRAM and flash memories as well as emerging device concepts Semiconductor memory is a good example of the full custom design that applies various analog and logic circuits to utilize the memory cell s device physics Critical physical effects that include tunneling hot electron injection charge trapping Flash memory are discussed in detail Emerging memories like FRAM PRAM and ReRAM that depend on magnetization electron spin alignment ferroelectric effect built in potential well quantum effects and thermal melting are also described CMOS Processors and Memories is a must for anyone serious about circuit design for

future computing technologies The book is written by top notch international experts in industry and academia It can be used in graduate course curriculum

□□□□□□□□□□□□□□□□ Hisa Ando,2011-06-24 LSI CONTENTS **IEEE Circuits & Devices**,1993 **CMOS Logic Circuit Design** John P. Uyemura,1999-02-28 This is an up to date treatment of the analysis and design of CMOS integrated digital logic circuits The self contained book covers all of the important digital circuit design styles found in modern CMOS chips emphasizing solving design problems using the various logic styles available in CMOS

Flip-Flop Design in Nanometer CMOS Massimo Alioto,Elio Consoli,Gaetano Palumbo,2014-10-14 This book provides a unified treatment of Flip Flop design and selection in nanometer CMOS VLSI systems The design aspects related to the energy delay tradeoff in Flip Flops are discussed including their energy optimal selection according to the targeted application and the detailed circuit design in nanometer CMOS VLSI systems Design strategies are derived in a coherent framework that includes explicitly nanometer effects including leakage layout parasitics and process voltage temperature variations as main advances over the existing body of work in the field The related design tradeoffs are explored in a wide range of applications and the related energy performance targets A wide range of existing and recently proposed Flip Flop topologies are discussed Theoretical foundations are provided to set the stage for the derivation of design guidelines and emphasis is given on practical aspects and consequences of the presented results Analytical models and derivations are introduced when needed to gain an insight into the inter dependence of design parameters under practical constraints This book serves as a valuable reference for practicing engineers working in the VLSI design area and as text book for senior undergraduate graduate and postgraduate students already familiar with digital circuits and timing Design and Optimization of Low-power CMOS Logic Using Logical Effort Model with Slope Correction Chengcheng Wang,2009

**Circuit Design for CMOS VLSI** John Paul Uyemura,1992 The field of CMOS integrated circuits has reached a level of maturity where it is now a mainstream technology for high density digital system designs This volume deals with circuit design in an integrated CMOS environment Emphasis is placed on understanding the operation performance and design o

*Digital CMOS Circuit Design* Silvia Annaratone,2012-12-06 *CMOS VLSI Design* Neil H. E. Weste,David F. Harris,2005 Details techniques for the design of complex and high performance CMOS Systems on Chip This edition explains practices of chip design covering transistor operation CMOS gate design fabrication and layout at level accessible to anyone with an elementary knowledge of digital electronics CMOS VLSI Design : A circuits and systems perspective Neil H.E.

Weste,David Harris,2015 The fourth edition of the best selling text details the modern techniques for the design of complex and high performance CMOS systems on a chip Covering the fundamentals of CMOS design from the digital systems level to the circuit level this book explains the fundamental principles and is a guide to good design practices **Principles of**

**CMOS VLSI Design** Neil H. E. Weste,Kamran Eshraghian,1993 With this revision Weste conveys an understanding of CMOS technology circuit design layout and system design sufficient to the designer The book deals with the technology down to the

layout level of detail thereby providing a bridge from a circuit to a form that may be fabricated

**High Speed CMOS Design Styles** Kerry Bernstein, K.M. Carrig, Christopher M. Durham, Patrick R. Hansen, David Hogenmiller, Edward J. Nowak, Norman J. Rohrer, 2012-12-06 High Speed CMOS Design Styles is written for the graduate level student or practicing engineer who is primarily interested in circuit design. It is intended to provide practical reference or horse sense to mechanisms typically described with a more academic slant. This book is organized so that it can be used as a textbook or as a reference book. High Speed CMOS Design Styles provides a survey of design styles in use in industry specifically in the high speed microprocessor design community. Logic circuit structures I/O and interface clocking and timing schemes are reviewed and described. Characteristics sensitivities and idiosyncrasies of each are highlighted. High Speed CMOS Design Styles also pulls together and explains contributors to performance variability that are associated with process applications conditions and design. Rules of thumb and practical references are offered. Each of the general circuit families is then analyzed for its sensitivity and response to this variability. High Speed CMOS Design Styles is an excellent source of ideas and a compilation of observations that highlight how different approaches trade off critical parameters in design and process space.

**Ultra High-Speed CMOS Circuits** Sam Gharavi, Babak Heydari, 2011-09-25 The book covers the CMOS based millimeter wave circuits and devices and presents methods and design techniques to use CMOS technology for circuits operating beyond 100 GHz. Coverage includes a detailed description of both active and passive devices including modeling techniques and performance optimization. Various mm wave circuit blocks are discussed emphasizing their design distinctions from low frequency design methodologies. This book also covers a device oriented circuit design technique that is essential for ultra high speed circuits and gives some examples of device circuit co design that can be used for mm wave technology.

**Handbook of Digital CMOS Technology, Circuits, and Systems** Karim Abbas, 2020-01-14 This book provides a comprehensive reference for everything that has to do with digital circuits. The author focuses equally on all levels of abstraction. He tells a bottom up story from the physics level to the finished product level. The aim is to provide a full account of the experience of designing fabricating understanding and testing a microchip. The content is structured to be very accessible and self contained allowing readers with diverse backgrounds to read as much or as little of the book as needed. Beyond a basic foundation of mathematics and physics the book makes no assumptions about prior knowledge. This allows someone new to the field to read the book from the beginning. It also means that someone using the book as a reference will be able to answer their questions without referring to any external sources.

**Low-Power CMOS Circuits** Christian Piguet, 2018-10-03 The power consumption of microprocessors is one of the most important challenges of high performance chips and portable devices. In chapters drawn from Piguet's recently published Low Power Electronics Design Low Power CMOS Circuits Technology Logic Design and CAD Tools addresses the design of low power circuitry in deep submicron technologies. It provides a focused reference for specialists involved in designing low power circuitry from transistors to logic

gates The book is organized into three broad sections for convenient access The first examines the history of low power electronics along with a look at emerging and possible future technologies It also considers other technologies such as nanotechnologies and optical chips that may be useful in designing integrated circuits The second part explains the techniques used to reduce power consumption at low levels These include clock gating leakage reduction interconnecting and communication on chips and adiabatic circuits The final section discusses various CAD tools for designing low power circuits This section includes three chapters that demonstrate the tools and low power design issues at three major companies that produce logic synthesizers Providing detailed examinations contributed by leading experts Low Power CMOS Circuits Technology Logic Design and CAD Tools supplies authoritative information on how to design and model for high performance with low power consumption in modern integrated circuits It is a must read for anyone designing modern computers or embedded systems

**CMOS** R. Jacob Baker, 2008 This edition provides an important contemporary view of a wide range of analog digital circuit blocks the BSIM model data converter architectures and more The authors develop design techniques for both long and short channel CMOS technologies and then compare the two

**Low Power High Speed CMOS Multiplexer Design** Shyam Akashe, Khusbou Mishra, 2015 This book proposes the reversible logic Multiplexer and also demarcates between reversible and irreversible logic Multiplexers For power reduction in future computing technologies reversible logic is a very productive approach of logic synthesis The purpose of this book is to reduce power and area of 2 1 MUX 4 1 MUX and reversible logic while maintaining the viable performance The diverse configurations are designed using different topologies of 2 1 MUX and 4 1 MUX such as CMOS based MUX transmission gate and pass transistor The editors propose a new application of GDI Gate Diffusion Input circuits to Reversible logic multiplexer with its Garbage input and output The novel proposed design technique will consume less power than the other conventional gate Reversible logic circuit has displayed less power dissipation in recent years Additionally this GDI cell technique decreases the power of the circuit delay Power Delay Product PDP and it also compacts the frequency The device scaling is partial as the power dissipations is more optimized in terms of delay frequency jitter bandwidth power supply frequency and duty cycle of the signal and also establishes the noise of the circuit In the reversible logic design the GDI is efficient in lower delay low power and low leakage current

**Testing and Reliable Design of CMOS Circuits** Niraj K. Jha, Sandip Kundu, 2012-12-06 In the last few years CMOS technology has become increasingly dominant for realizing Very Large Scale Integrated VLSI circuits The popularity of this technology is due to its high density and low power requirement The ability to realize very complex circuits on a single chip has brought about a revolution in the world of electronics and computers However the rapid advancements in this area pose many new problems in the area of testing Testing has become a very time consuming process In order to ease the burden of testing many schemes for designing the circuit for improved testability have been presented These design for testability techniques have begun to catch the attention of chip manufacturers The trend is

towards placing increased emphasis on these techniques Another byproduct of the increase in the complexity of chips is their higher susceptibility to faults In order to take care of this problem we need to build fault tolerant systems The area of fault tolerant computing has steadily gained in importance Today many universities offer courses in the areas of digital system testing and fault tolerant computing Due to the importance of CMOS technology a significant portion of these courses may be devoted to CMOS testing This book has been written as a reference text for such courses offered at the senior or graduate level Familiarity with logic design and switching theory is assumed The book should also prove to be useful to professionals working in the semiconductor industry

**Nano-CMOS Circuit and Physical Design** Ban Wong, Anurag Mittal, Yu Cao, Greg W. Starr, 2005-04-08 Based on the authors expansive collection of notes taken over the years Nano CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing manufacturability and yield This innovative book covers process technology including sub wavelength optical lithography impact of process scaling on circuit and physical implementation and low power with leaky transistors and DFM yield and the impact of physical implementation

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