

RS-485 failsafe biasing: Old versus new transceivers

By Thomas Kugelstadt
Senior Applications Engineer

It is incredible that an industrial interface standard such as RS-485, having been around for 30 years, still appears obscure to many industrial-network designers. While there should be plenty of literature available explaining the standard fundamentals, the Texas Instruments (TI) application team continues to receive basic questions on a weekly basis, such as how to apply failsafe biasing to an idle bus.

Failsafe biasing refers to the technique of providing a differential voltage to a terminated, idle bus in order to maintain the receiver output of a bus transceiver in a logic-high state. This technique is commonly required when legacy transceiver designs are used for designing bus networks.

Legacy designs such as transceiver X in Table 1 possess a wide input sensitivity of ± 200 mV. This means that small input signals between $+200$ mV and -200 mV can turn the receiver output either high or low, thus making the output state indeterminate.

During a data transmission, the differential line voltage of a fully loaded bus is required to be higher than ± 1.5 V, which is well above the transceiver's input sensitivity. However, during a handover of bus access from one node to another, or during a transmission pause, the bus idles. Then the low-impedance termination resistors, connecting the two conductors of the differential signal pair with each other, cause the differential bus voltage to be 0 V, right in the middle of the transceiver's input sensitivity, which produces an indeterminate output.

Therefore, to keep the receiver outputs at a logic high during bus idling, a positive, differential failsafe voltage higher than a receiver's positive input threshold (V_{IT+}) must be applied to the bus.

Table 1 shows that the theoretically required failsafe levels decrease with the receiver's positive input threshold from one generation to the next. While transceiver X

requires a minimum of ± 200 mV of failsafe biasing, transceivers Y and Z can do without it as their positive input thresholds are below 0 V. Unfortunately, these values apply only in noise-free environments such as laboratories or the Earth's poles, and certainly not in the harsh environments of industrial factories where RS-485 networks are commonly installed.

Differential noise induced into the bus wires can falsely trigger a receiver input if the projected noise magnitude has not been included in the failsafe voltage calculation. Using a twisted-pair bus cable helps to convert noise induced along the cable run into common-mode noise. This noise is then rejected by the receiver's differential input. However, cable irregularities as well as noise induced at the bus node connectors might contribute to differential noise that cannot be rejected by a receiver.

Figure 1 on the next page shows that when a noise signal is superimposed onto the positive input threshold levels of transceivers X and Y, the minimum hysteresis voltage determines at which noise level the receiver output will assume the wrong logic state. Table 1, in which the receiver parameters have been extracted from different datasheets, gives a minimum hysteresis level only for transceiver Z. For the two older transceivers, X and Y, only typical hysteresis values are provided. In a situation such as determining the minimum failsafe value for a worst-case scenario, typical values are meaningless. In fact, the TI application team has measured minimum hysteresis voltages for both transceivers X and Y that were nearly half the specified typical values.

Furthermore, there is the possibility that for a given transceiver the hysteresis window might be located anywhere between the positive and negative input thresholds. Hence, for a worst-case calculation, one must assume that the hysteresis window is at the uppermost positive

Table 1. Receiver input sensitivities of first-, second-, and third-generation (X, Y, and Z) transceivers

TRANSCIVER	POSITIVE-GOING INPUT THRESHOLD VOLTAGE, V_{IT+} (mV)			NEGATIVE-GOING INPUT THRESHOLD VOLTAGE, V_{IT-} (mV)			INPUT HYSTERESIS VOLTAGE, V_{HYS} (mV)			RECEIVER OUTPUT IS INDETERMINATE WHEN
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
X (SN65LBC126)			200	-200				50		$-0.2 \text{ V} < V_{DIF} < 0.2 \text{ V}$
Y (SN65HVD12)			-10	-200				35		$-0.2 \text{ V} < V_{DIF} < 0.01 \text{ V}$
Z (SN65HVD72)		-70	-20	-200	-150		50	80		$-0.2 \text{ V} < V_{DIF} < 0.07 \text{ V}$

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