Automatic Placement and Routing using Cadence Encounter

6.375 Tutorial 5
February 12, 2007

In this tutorial you will gain experience using Cadence Encounter to perform automatic placement and routing. A place+route tool takes a gate-level netlist as input and first determines how each gate should be placed on the chip. It uses several heuristic algorithms to group related gates together and thus hopefully minimize routing congestion and wire delay. Place+route tools will focus their effort on minimizing the delay through the critical path. To this end, these tools can resize gates, insert new buffers, and even perform local resynthesis. Place+route tools often have additional algorithms to help reduce area for non-critical paths. After placement, the place+route tool will attempt to route the design while minimizing wire delay. Place+route tools often include additional facilities for clock tree synthesis, power routing, and block level floorplanning. Figure 1 shows how Encounter fits into the 6.375 toolflow.

The following documentation is located in the course locker (`/mit/6.375/doc`) and provides additional information about Encounter and the Tower 0.18 µm Standard Cell Library.

- `tsl-180nm-sc-databook.pdf` - Databook for Tower 0.18 µm Standard Cell Library
- `encounter-user-guide.pdf` - Encounter user guide
- `encounter-command-line-ref.pdf` - Encounter text command reference
- `encounter-menu-ref.pdf` - Encounter GUI reference

Getting started

Before using the 6.375 toolflow you must add the course locker and run the course setup script with the following two commands.

```
% add 6.375
% source /mit/6.375/setup.csh
```

For this tutorial we will be using an unpipelined SMIPSv1 processor as our example RTL design. You should create a working directory and checkout the SMIPSv1 example project from the course CVS repository using the following commands.

```
% mkdir tut5
% cd tut5
% cvs checkout examples/smipsv1-1stage-v
% cd examples/smipsv1-1stage-v
```

Before starting, take a look at the subdirectories in the `smipsv1-1stage-v` project directory. Figure 2 shows the system diagram which is implemented by the example code. When pushing designs through the physical toolflow we will often refer to the *core*. The core module contains everything which will be on-chip, while blocks outside the core are assume to be off-chip. For this tutorial we are assuming that the processor and a *combinational* memory are located within the core. A combinational memory means that the read address is specified at the beginning of the cycle, and

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Table of Contents Automatic Placement And Routing Using Cadence Encounter

1. Understanding the eBook Automatic Placement And Routing Using Cadence Encounter
    - The Rise of Digital Reading Automatic Placement And Routing Using Cadence Encounter
    - Advantages of eBooks Over Traditional Books
2. Identifying Automatic Placement And Routing Using Cadence Encounter
    - Exploring Different Genres
    - Considering Fiction vs. Non-Fiction
    - Determining Your Reading Goals
3. Choosing the Right eBook Platform
    - Popular eBook Platforms
    - Features to Look for in an Automatic Placement And Routing Using Cadence Encounter
    - User-Friendly Interface
4. Exploring eBook Recommendations from Automatic Placement And Routing Using Cadence Encounter
    - Personalized Recommendations
    - Automatic Placement And Routing Using Cadence Encounter User Reviews and Ratings

- Automatic Placement And Routing Using Cadence Encounter and Bestseller Lists

5. Accessing Automatic Placement And Routing Using Cadence Encounter Free and Paid eBooks
   - Automatic Placement And Routing Using Cadence Encounter Public Domain eBooks
   - Automatic Placement And Routing Using Cadence Encounter eBook Subscription Services
   - Automatic Placement And Routing Using Cadence Encounter Budget-Friendly Options
6. Navigating Automatic Placement And Routing Using Cadence Encounter eBook Formats
   - ePub, PDF, MOBI, and More
   - Automatic Placement And Routing Using Cadence Encounter Compatibility with Devices
   - Automatic Placement And Routing Using Cadence Encounter Enhanced eBook Features
7. Enhancing Your Reading Experience
   - Adjustable Fonts and Text Sizes of Automatic Placement And Routing Using Cadence Encounter
   - Highlighting and Note-Taking Automatic Placement And Routing Using Cadence Encounter
   - Interactive Elements Automatic Placement And Routing Using Cadence Encounter
8. Staying Engaged with Automatic Placement And Routing Using Cadence Encounter
   - Joining Online Reading Communities
   - Participating in Virtual Book Clubs
   - Following Authors and Publishers Automatic Placement And Routing Using Cadence Encounter
9. Balancing eBooks and Physical Books Automatic Placement And Routing Using Cadence Encounter
   - Benefits of a Digital Library
   - Creating a Diverse Reading Collection Automatic Placement And Routing Using Cadence Encounter
10. Overcoming Reading Challenges
    - Dealing with Digital Eye Strain
    - Minimizing Distractions
    - Managing Screen Time
11. Cultivating a Reading Routine Automatic Placement And Routing Using Cadence Encounter
    - Setting Reading Goals Automatic Placement And Routing Using Cadence Encounter
    - Carving Out Dedicated Reading Time
12. Sourcing Reliable Information of Automatic Placement And Routing Using Cadence Encounter
    - Fact-Checking eBook Content of Automatic Placement And Routing Using Cadence Encounter
    - Distinguishing Credible Sources

13. Promoting Lifelong Learning
    - Utilizing eBooks for Skill Development
    - Exploring Educational eBooks
14. Embracing eBook Trends
    - Integration of Multimedia Elements
    - Interactive and Gamified eBooks

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