

VHDL Code for Making a 16-to-1 MUX from 4-to-1 MUXes

- Here is complete code for a 4-to-1 MUX, using a selected signal assignment. (Could use conditional signal assignment instead.)

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;

ENTITY mux4to1 IS
    PORT ( w0, w1, w2, w3 : IN    STD_LOGIC ;
          s                : IN    STD_LOGIC_VECTOR(1 DOWNTO 0) ;
          f                : OUT   STD_LOGIC ) ;
END mux4to1 ;

ARCHITECTURE Behavior OF mux4to1 IS
BEGIN
    WITH s SELECT
        f <=  w0 WHEN "00",
              w1 WHEN "01",
              w2 WHEN "10",
              w3 WHEN OTHERS ;
END Behavior ;
```

Aes Vhdl Code

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